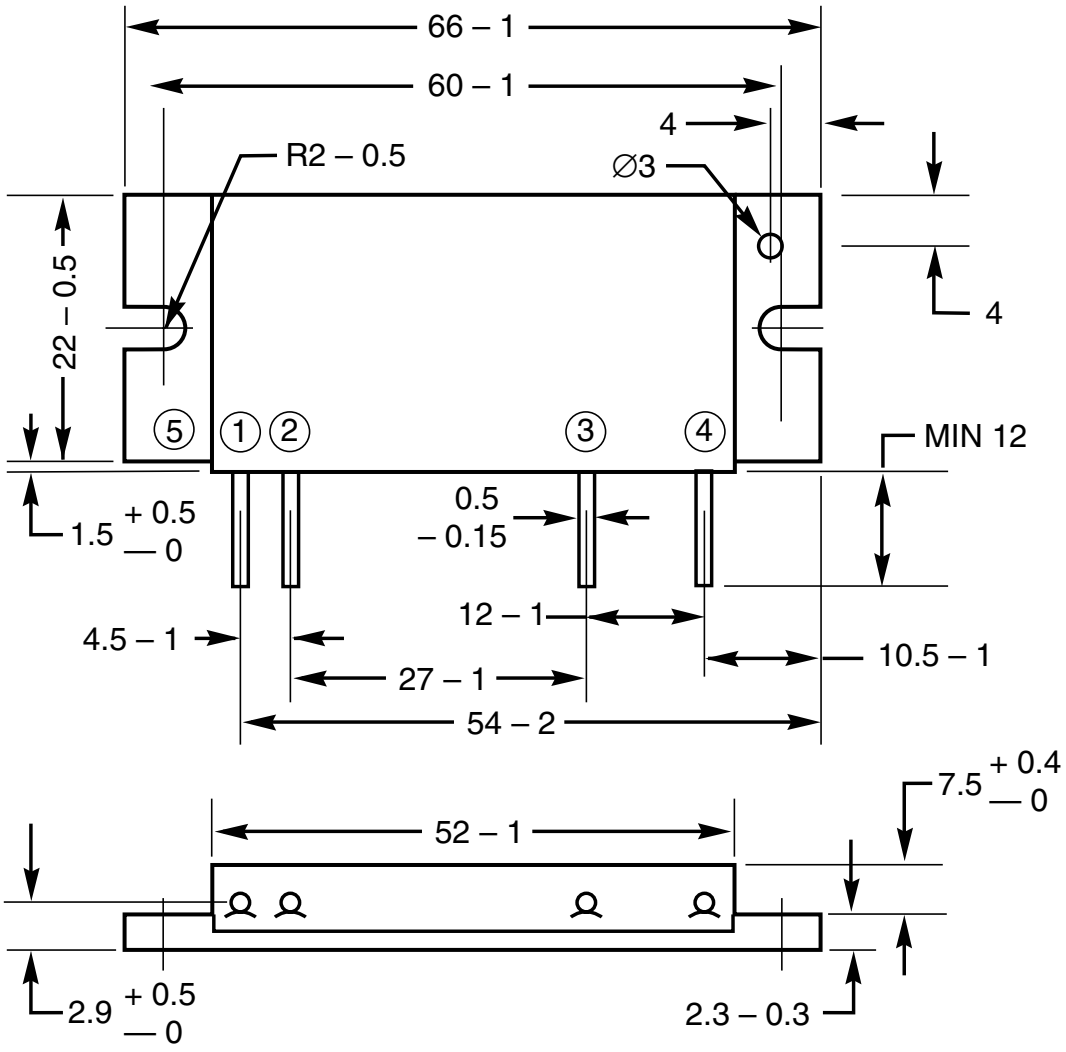
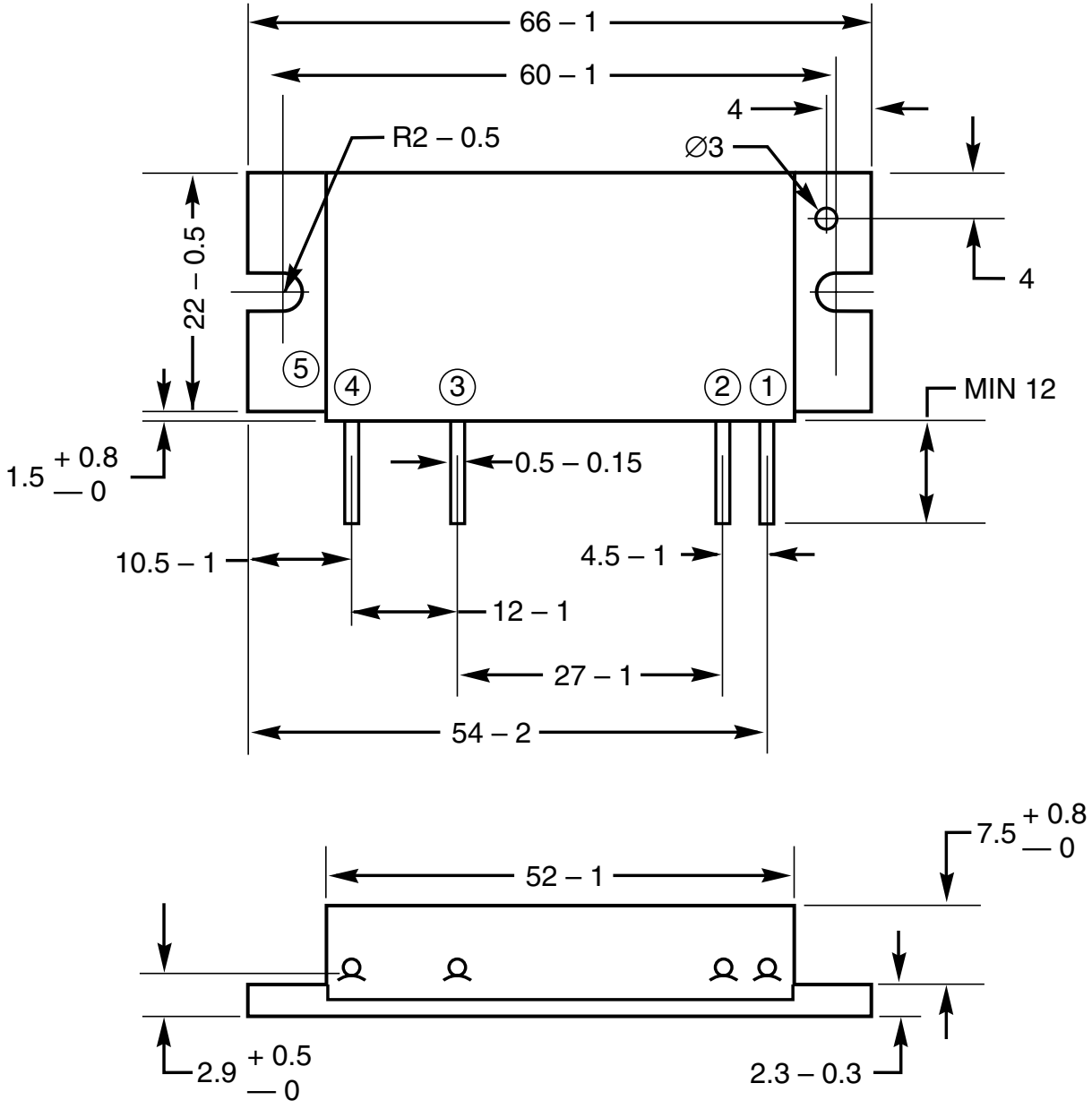
H2



PIN:

① INPUT
② V_{CC1}
③ V_{CC2}
④ OUTPUT
⑤ GND

H2R

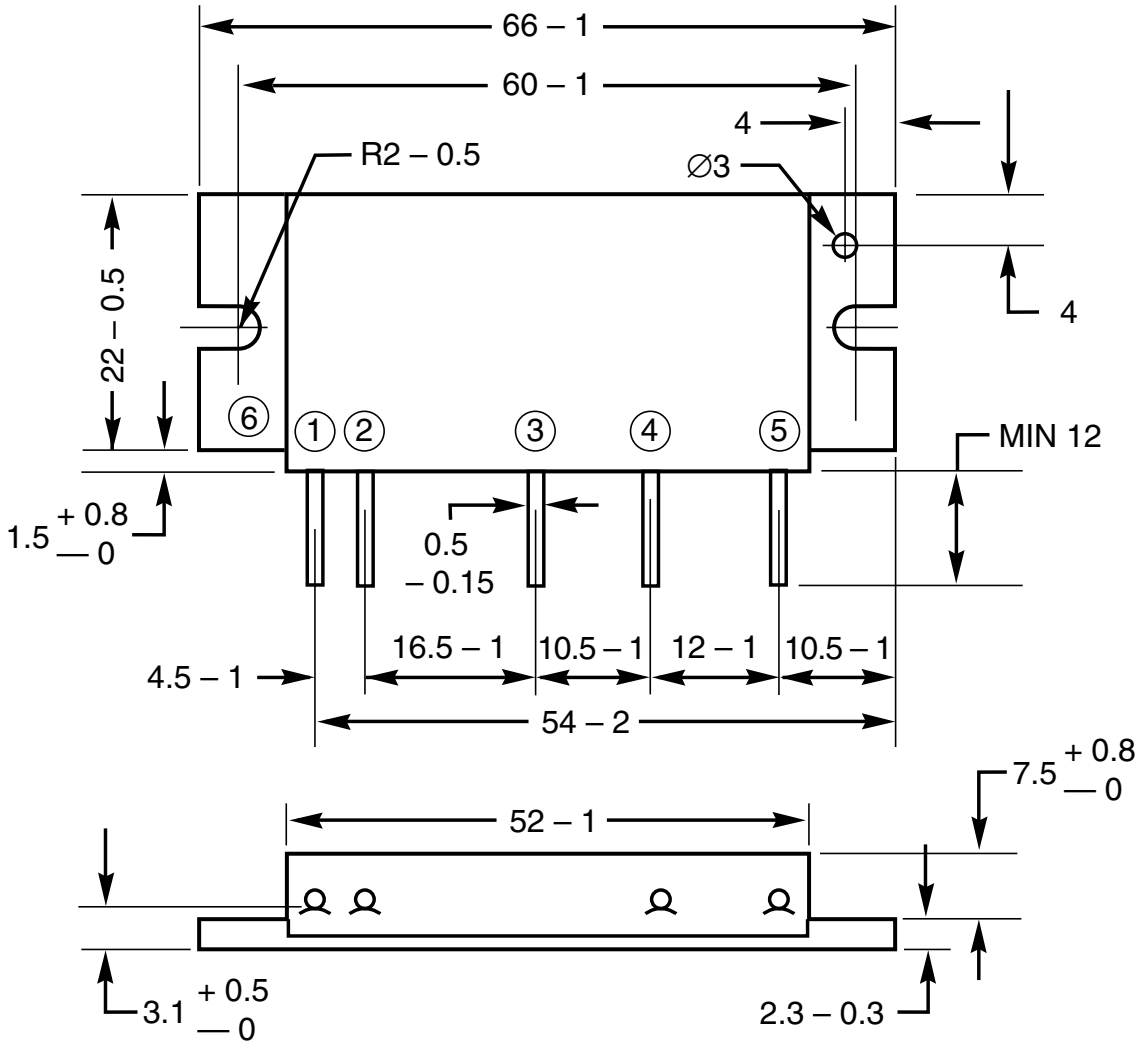


PIN:

① INPUT ③ V_{CC2} ⑤ GND

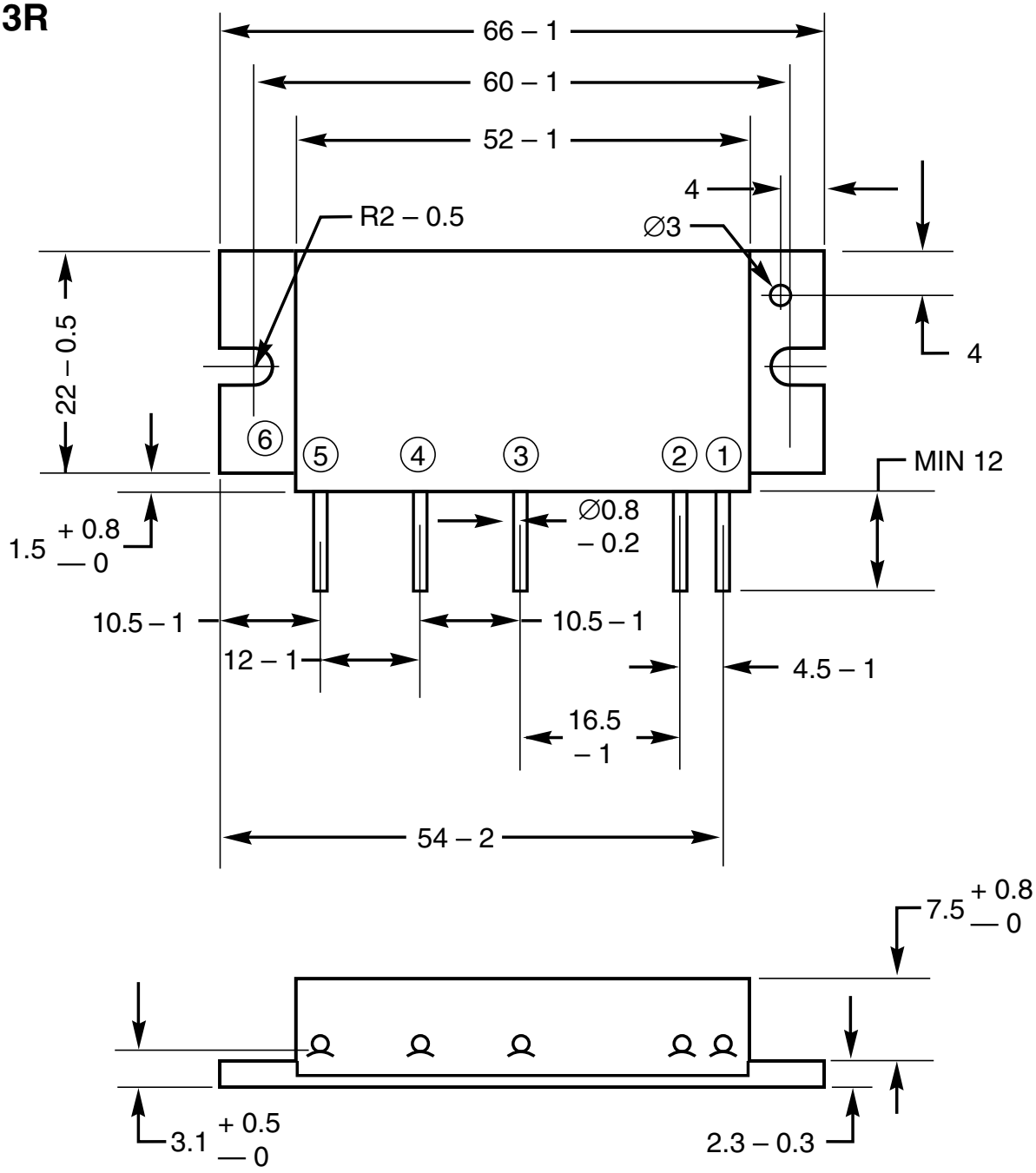
② V_{CC1} ④ OUTPUT

H3A,B,C



PIN:	A	B	C
①	INPUT	INPUT	INPUT
②	V_{CC1}	V_{CC1}	V_{BB}
③	V_{CC2}	V_{BB}	V_{CC1}
④	V_{CC3}	V_{CC2}	V_{CC2}
⑤	OUTPUT	OUTPUT	OUTPUT
⑥	GND	GND	GND

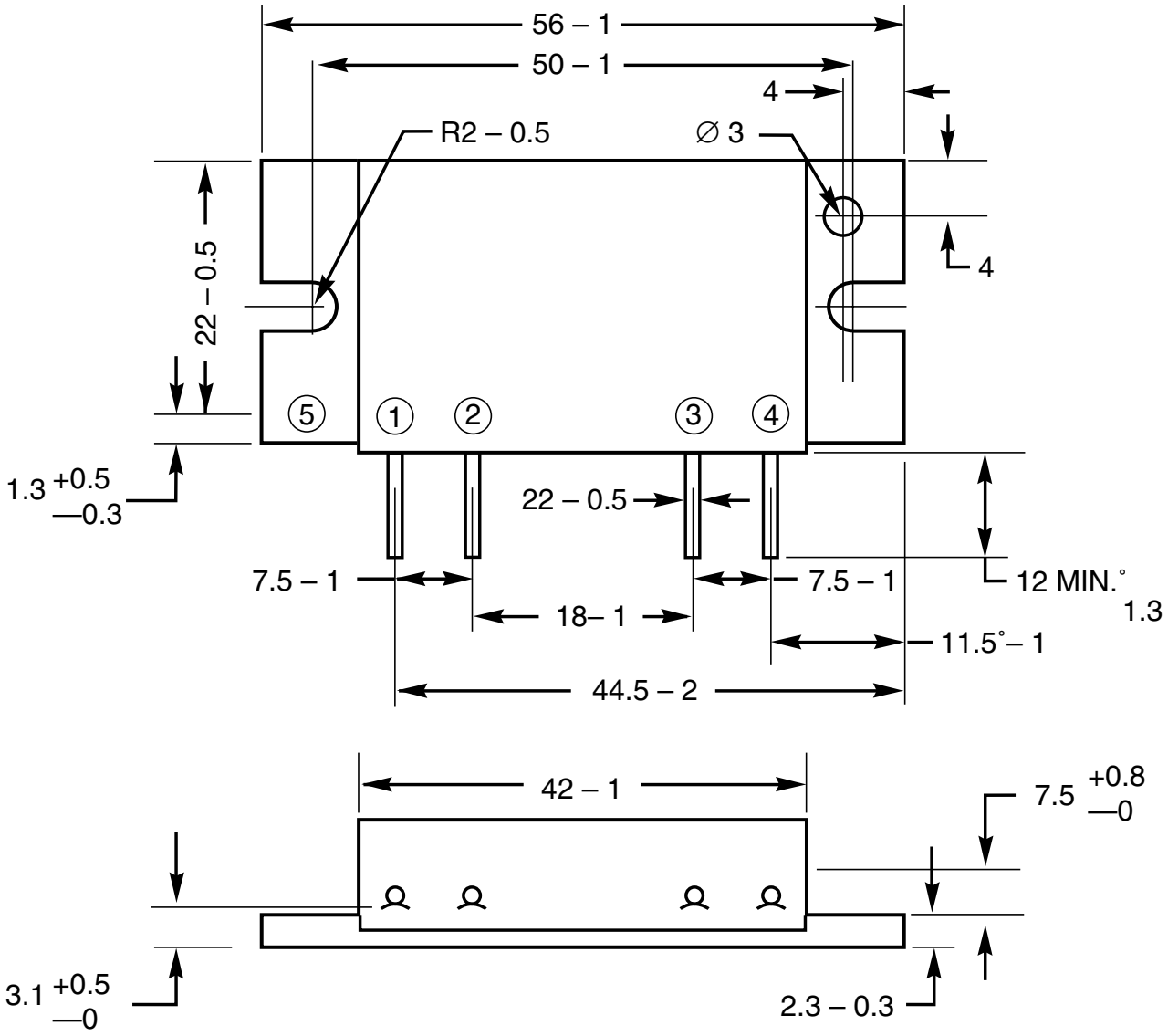
H3R



PIN:

① INPUT	③ V_{CC2}	⑤ OUTPUT
② V_{CC1}	④ V_{CC3}	⑥ GND

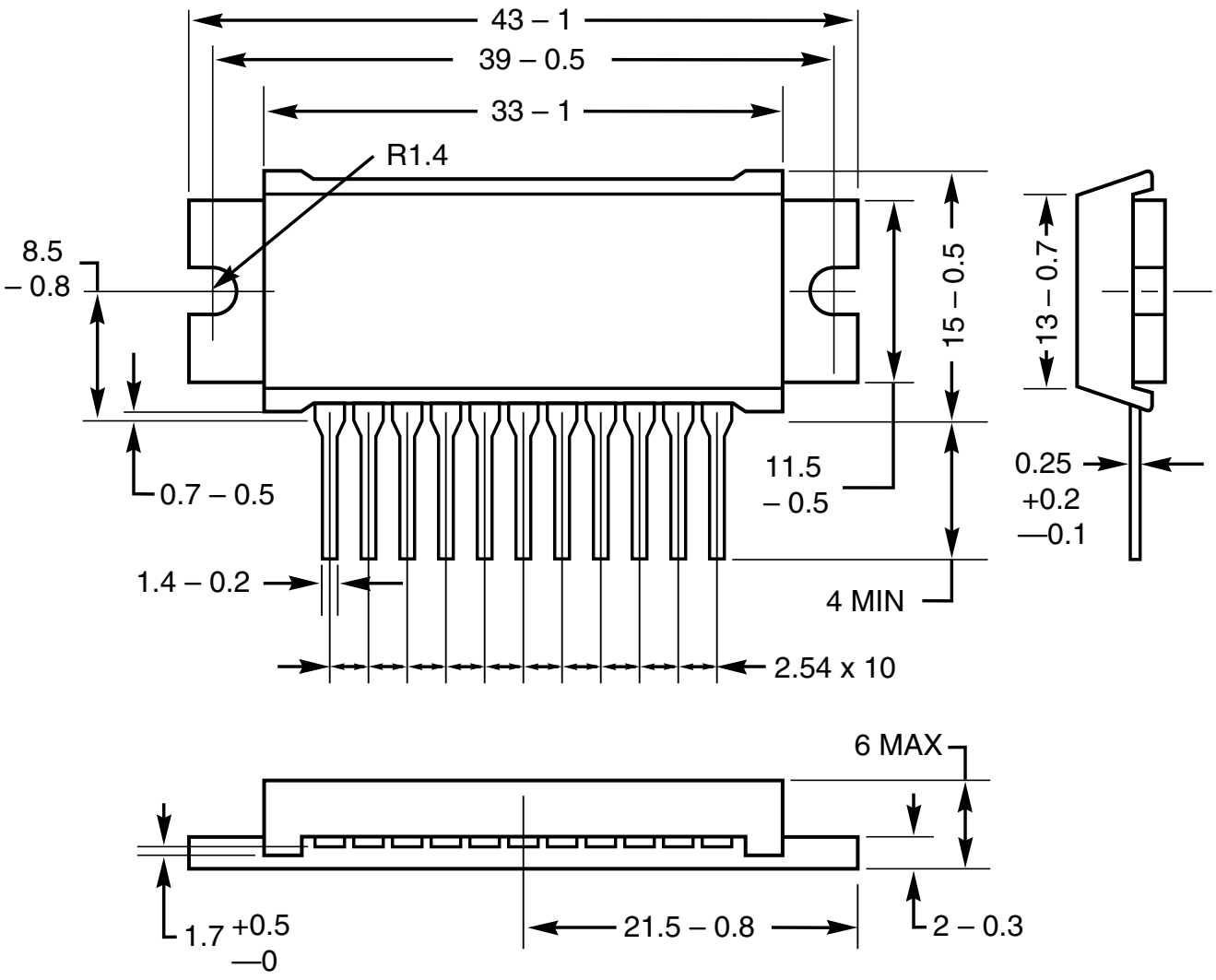
H6



PIN:

① INPUT
② V_{CC1}
③ V_{CC2}
④ OUTPUT
⑤ GND

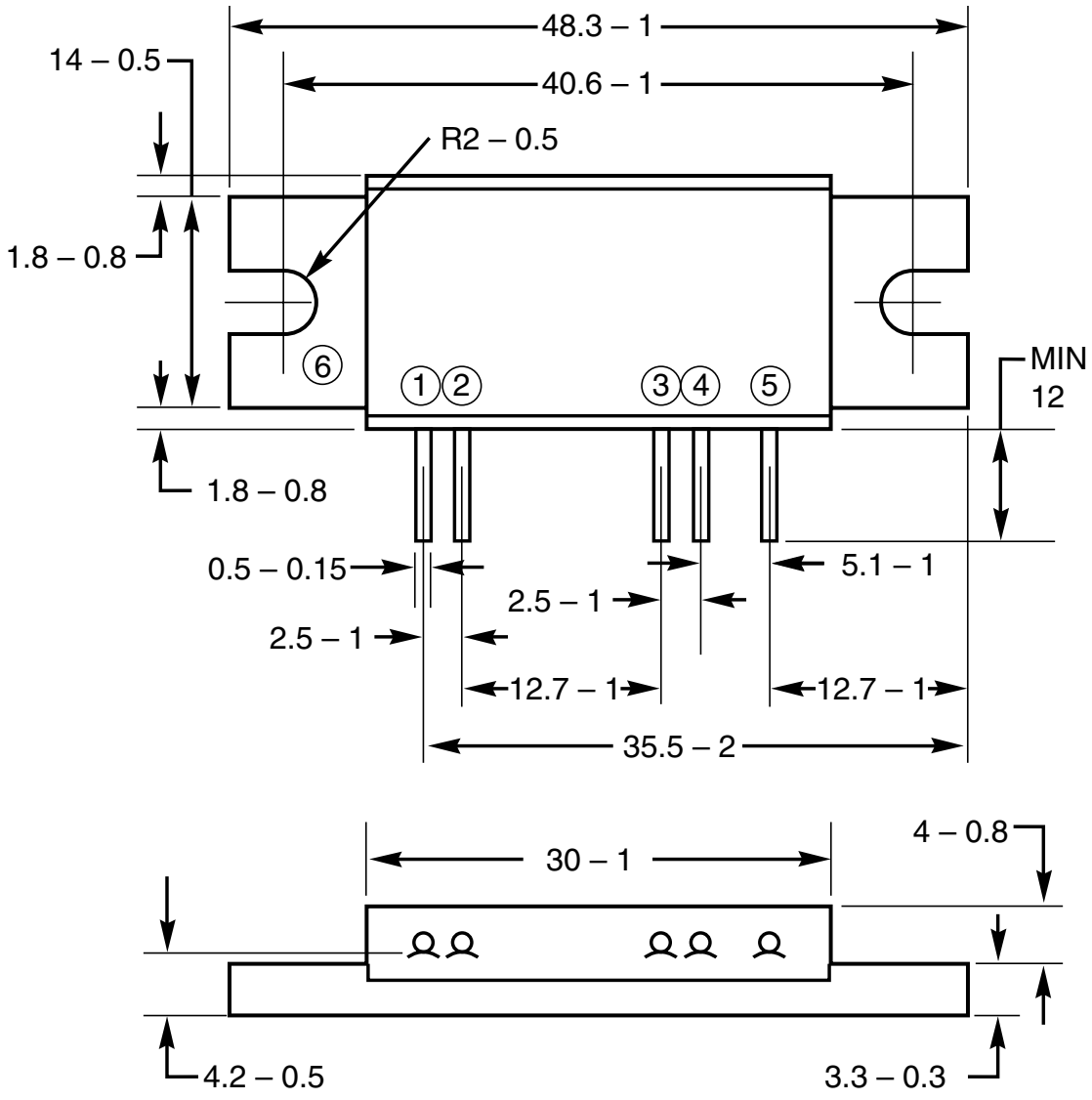
H8



PIN:

① INPUT	⑨ V_{CC2}
②~④ GND	⑩ GND
⑤ V_{CC1}	⑪ OUTPUT
⑥~⑧ GND	⑫ GND

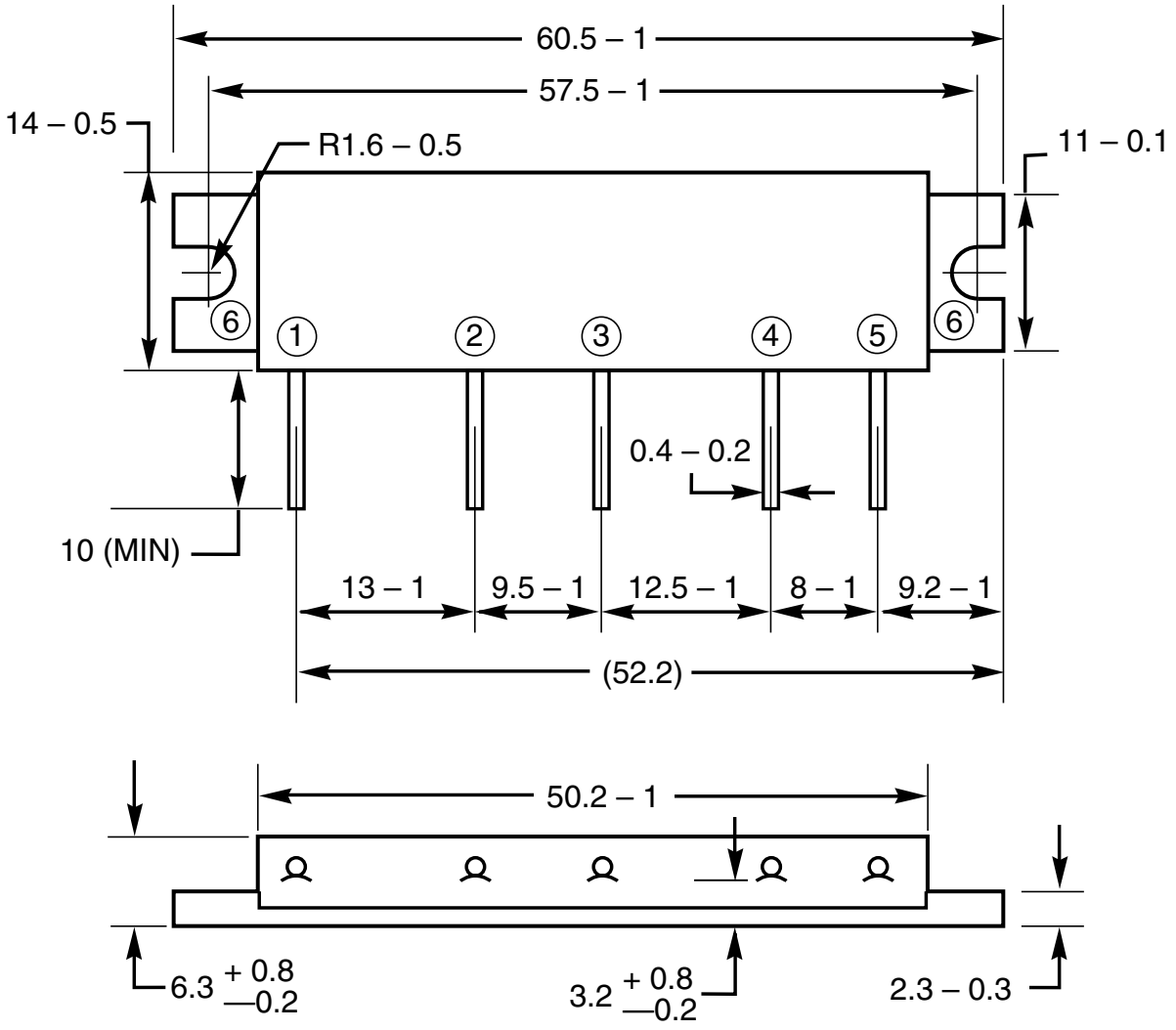
H10



PIN:

1. INPUT
2. V_{CC1}
3. V_{BB}
4. V_{CC2}
5. OUTPUT
6. GND

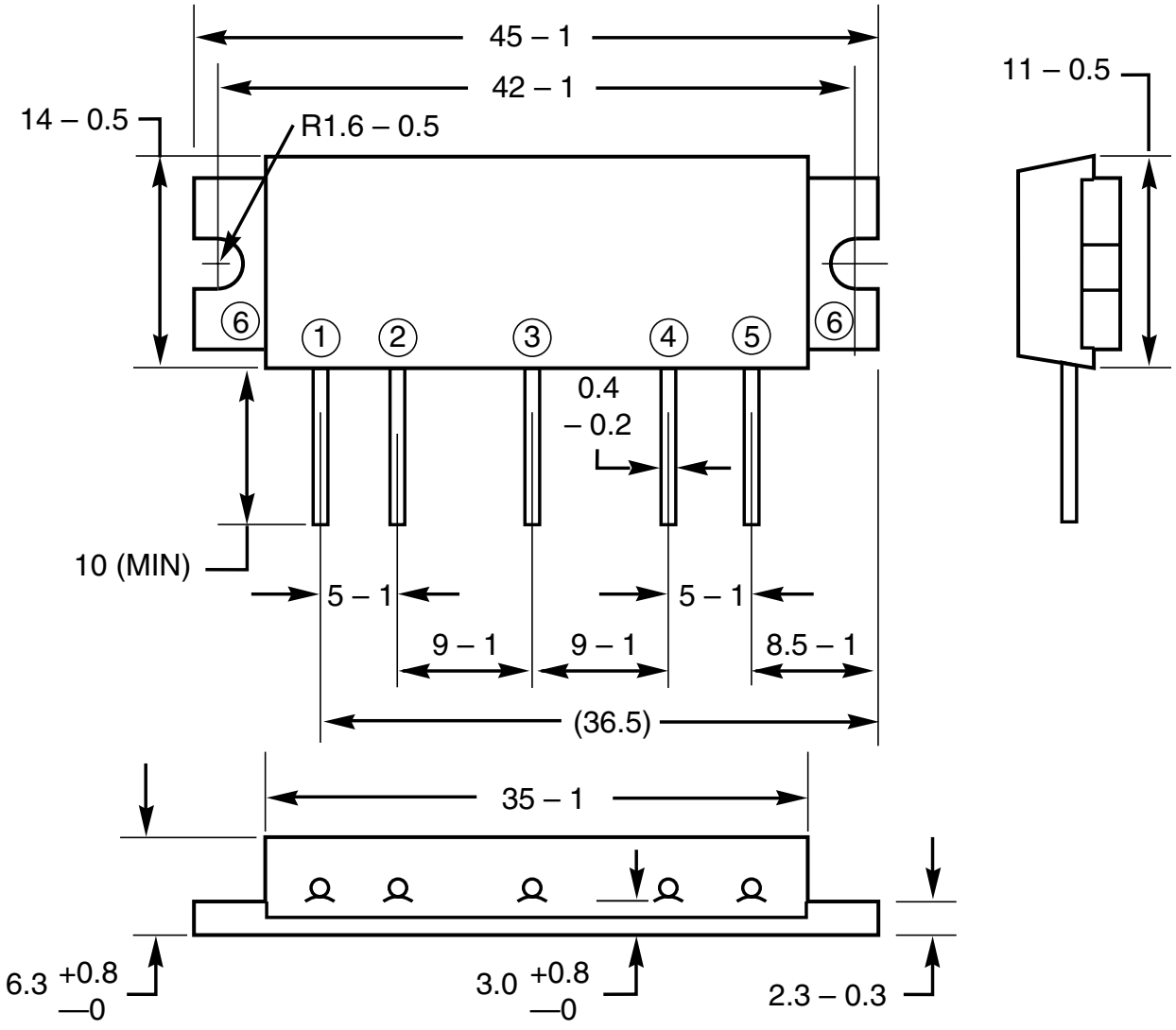
H11



PIN:

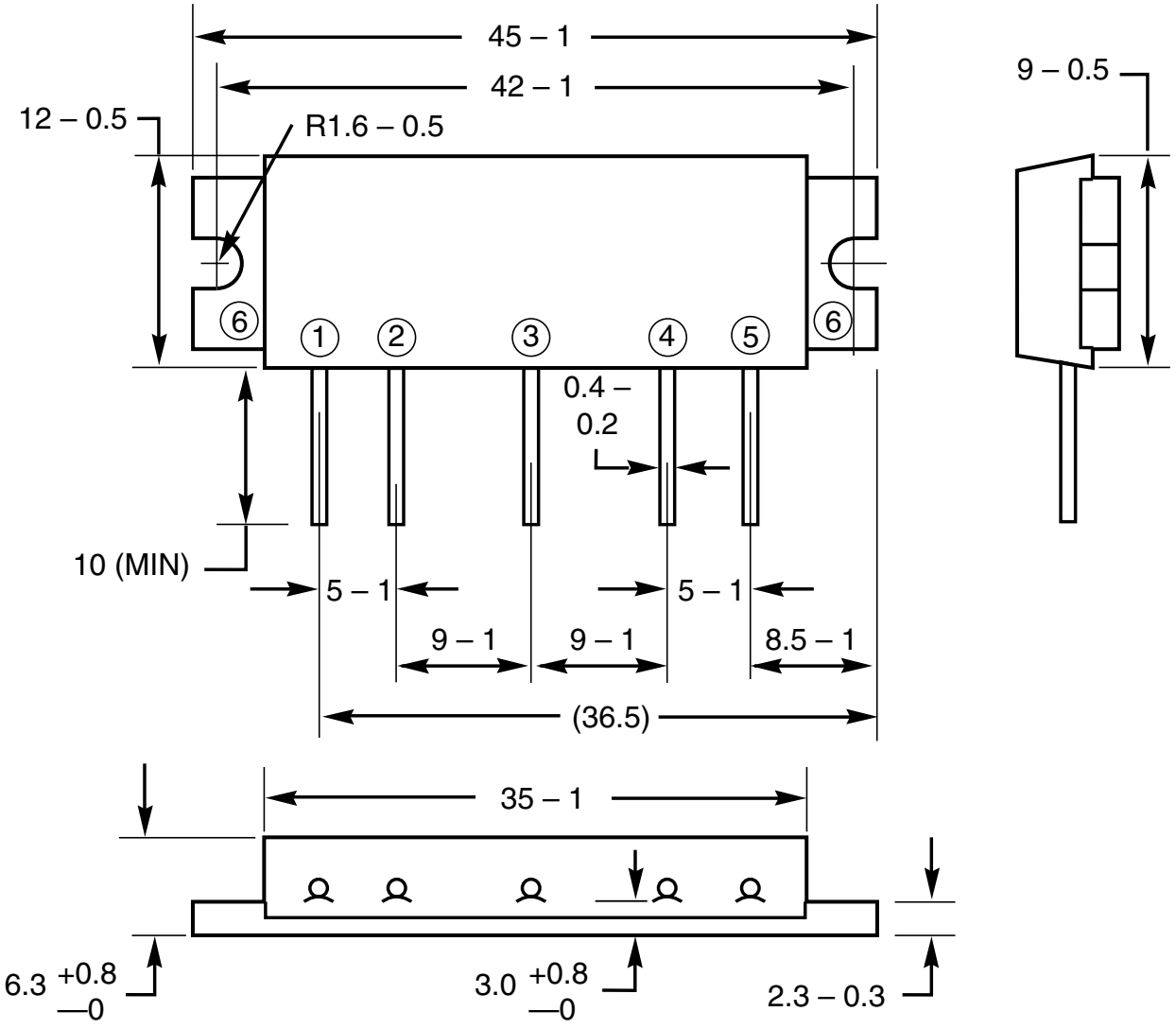
1. INPUT
2. V_{CC1}
3. V_{BB}
4. V_{CC2}
5. OUTPUT
6. GND

H12A,B



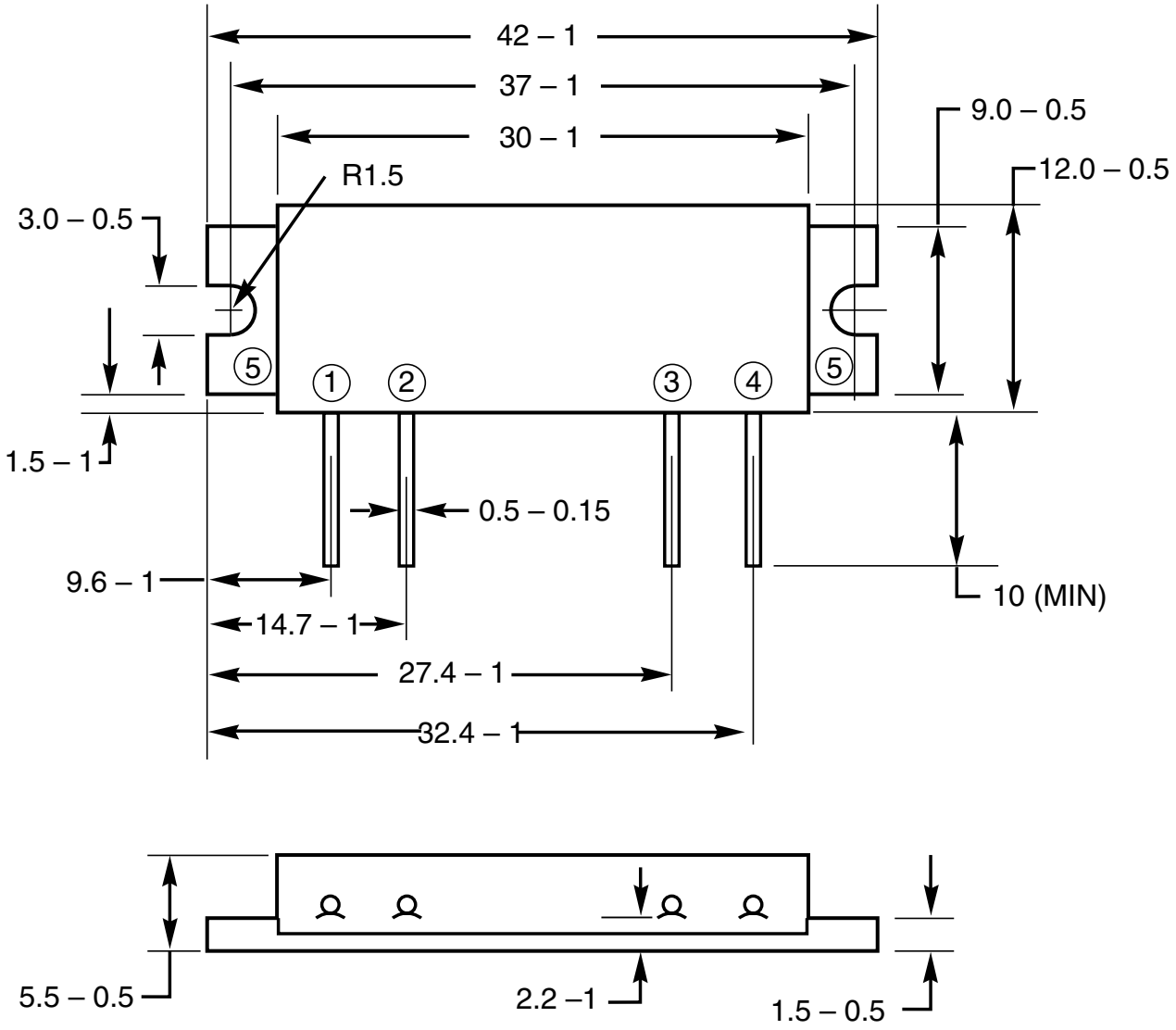
PIN:	A	B
①	INPUT	INPUT
②	V_{CC1}	V_{CC1}
③	V_{BB}	V_{CC2}
④	V_{CC2}	V_{CC3}
⑤	OUTPUT	OUTPUT
⑥	GND	GND

H13A,B



PIN:	A	B
①	INPUT	INPUT
②	V_{CC1}	V_{CC1}
③	V_{BB}	V_{CC2}
④	V_{CC2}	V_{CC3}
⑤	OUTPUT	OUTPUT
⑥	GND	GND

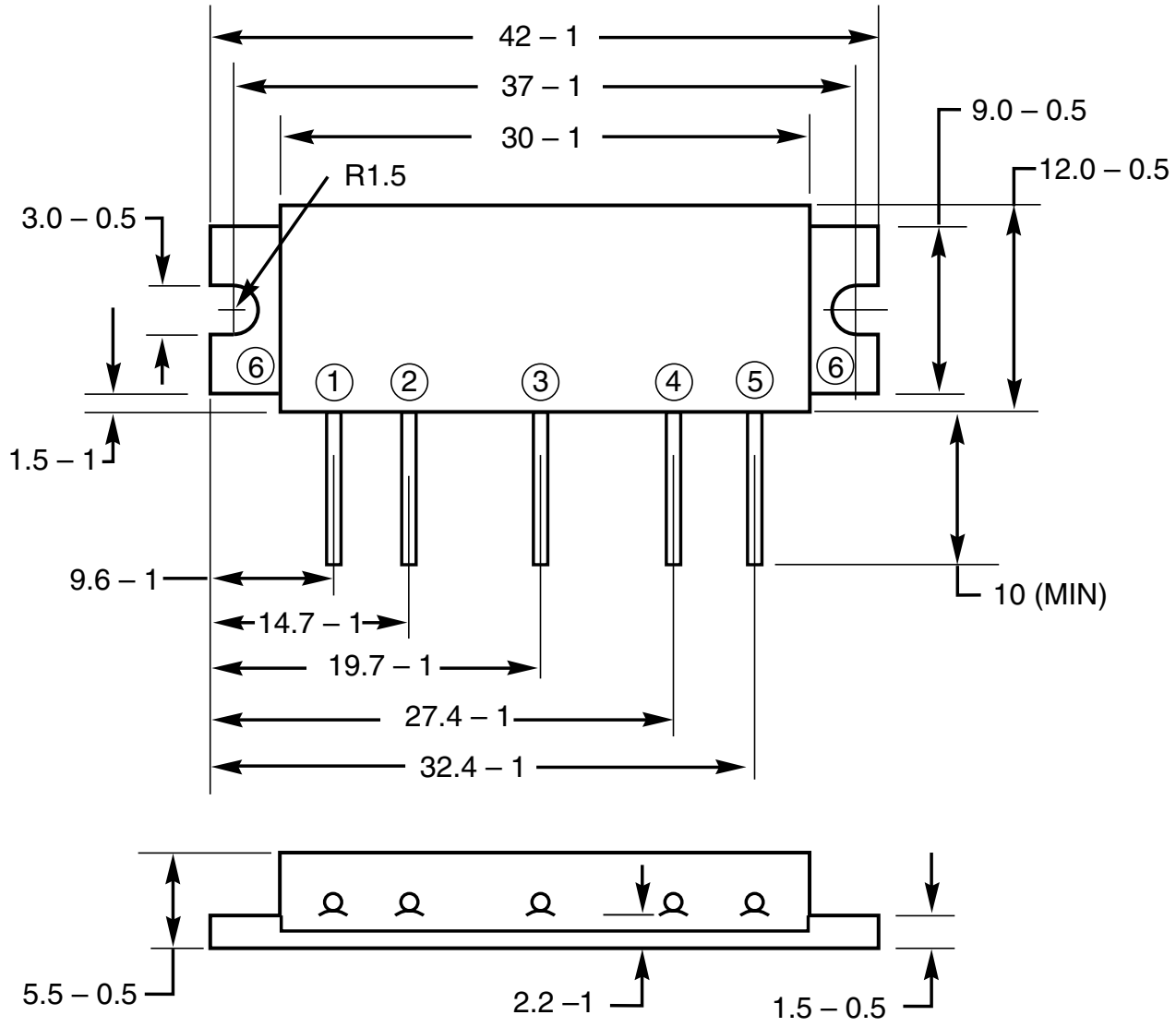
H14



PIN:

① INPUT
② V_{CC1}
③ V_{CC2}
④ OUTPUT
⑤ GND

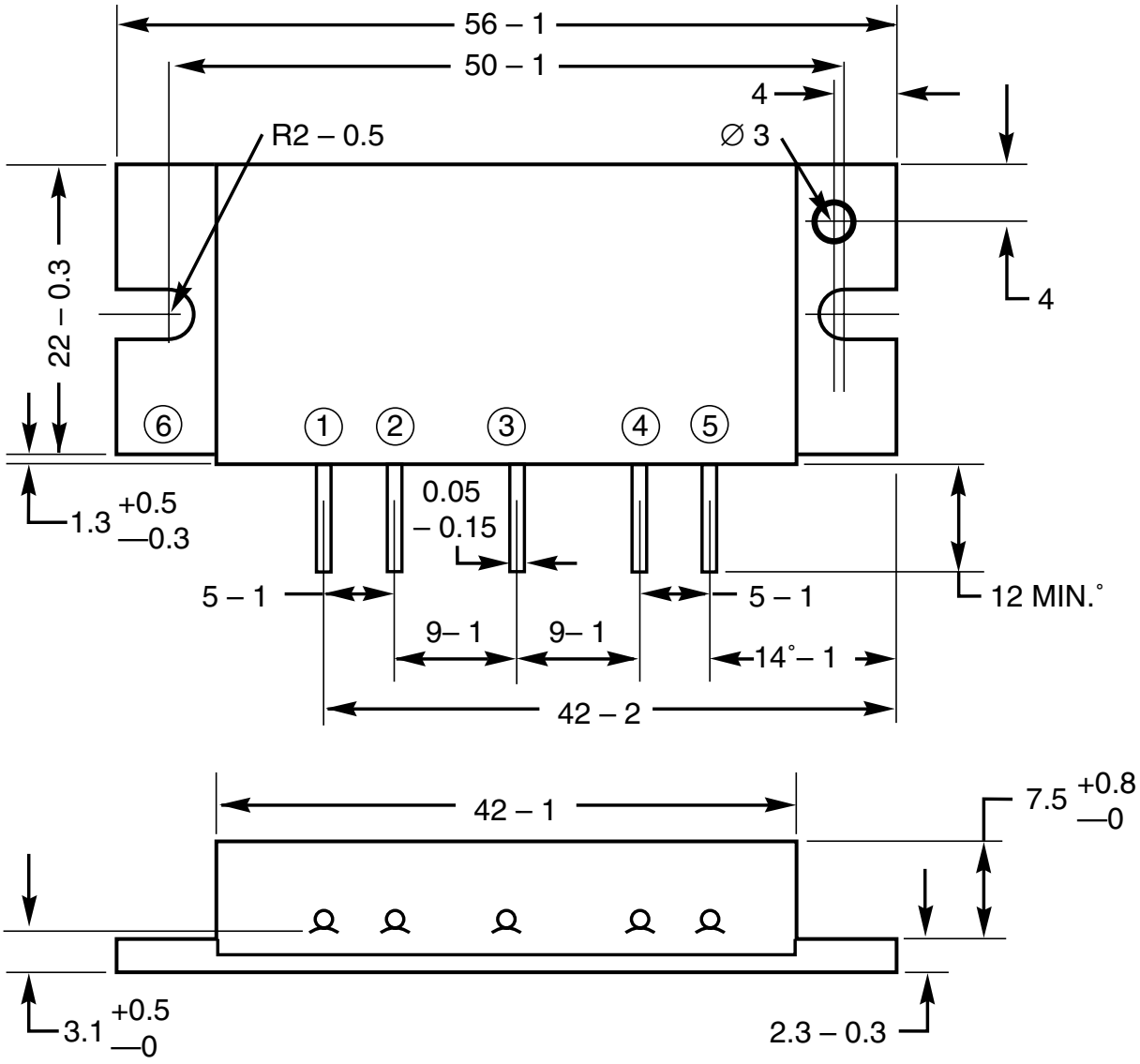
H15



PIN:

① INPUT
② V_{CC1}
③ V_{CC2}
④ V_{CC3}
⑤ OUTPUT
⑥ GND

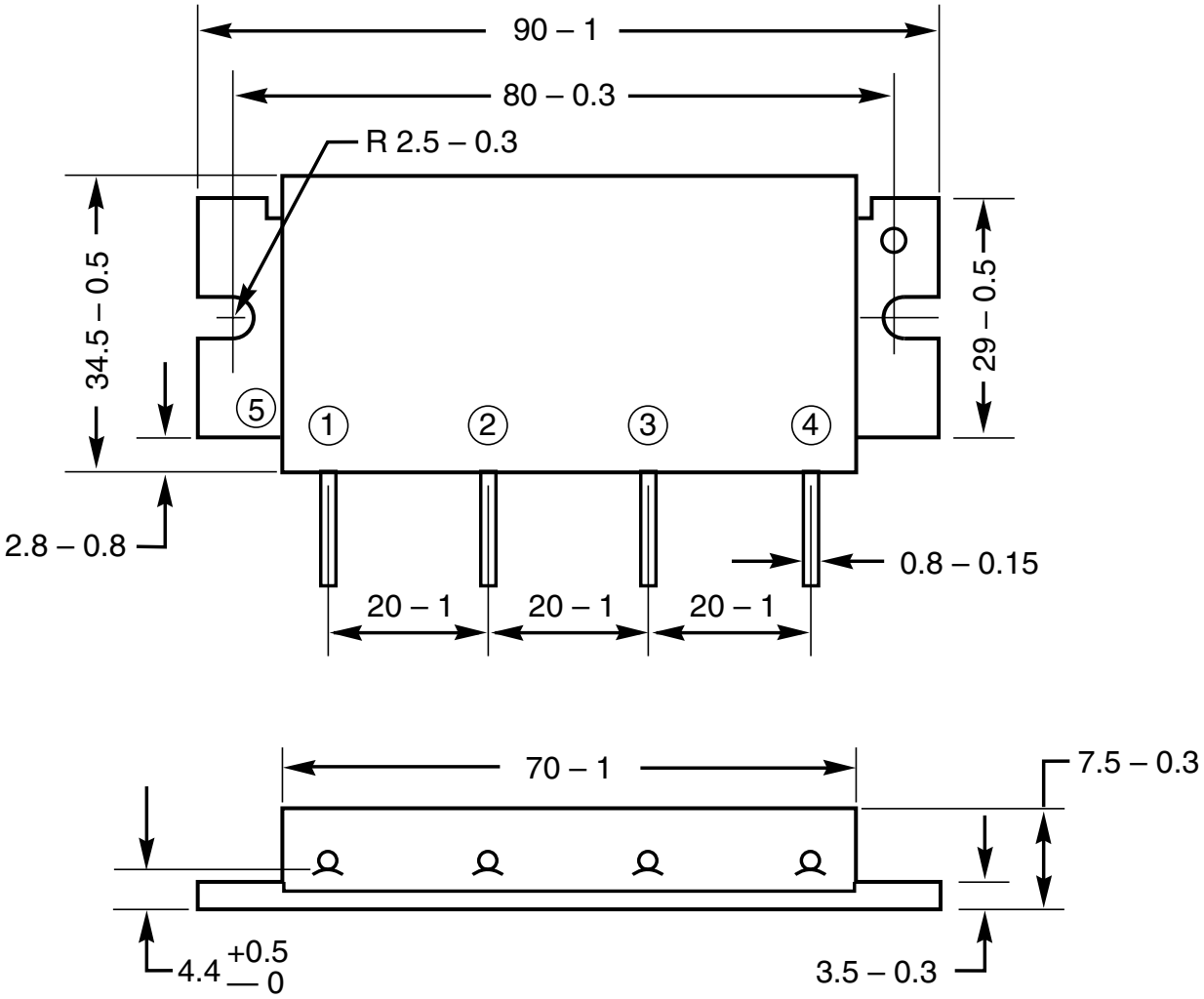
H16



PIN:

1. INPUT
2. V_{CC1}
3. V_{CC2}
4. V_{CC3}
5. OUTPUT
6. GND

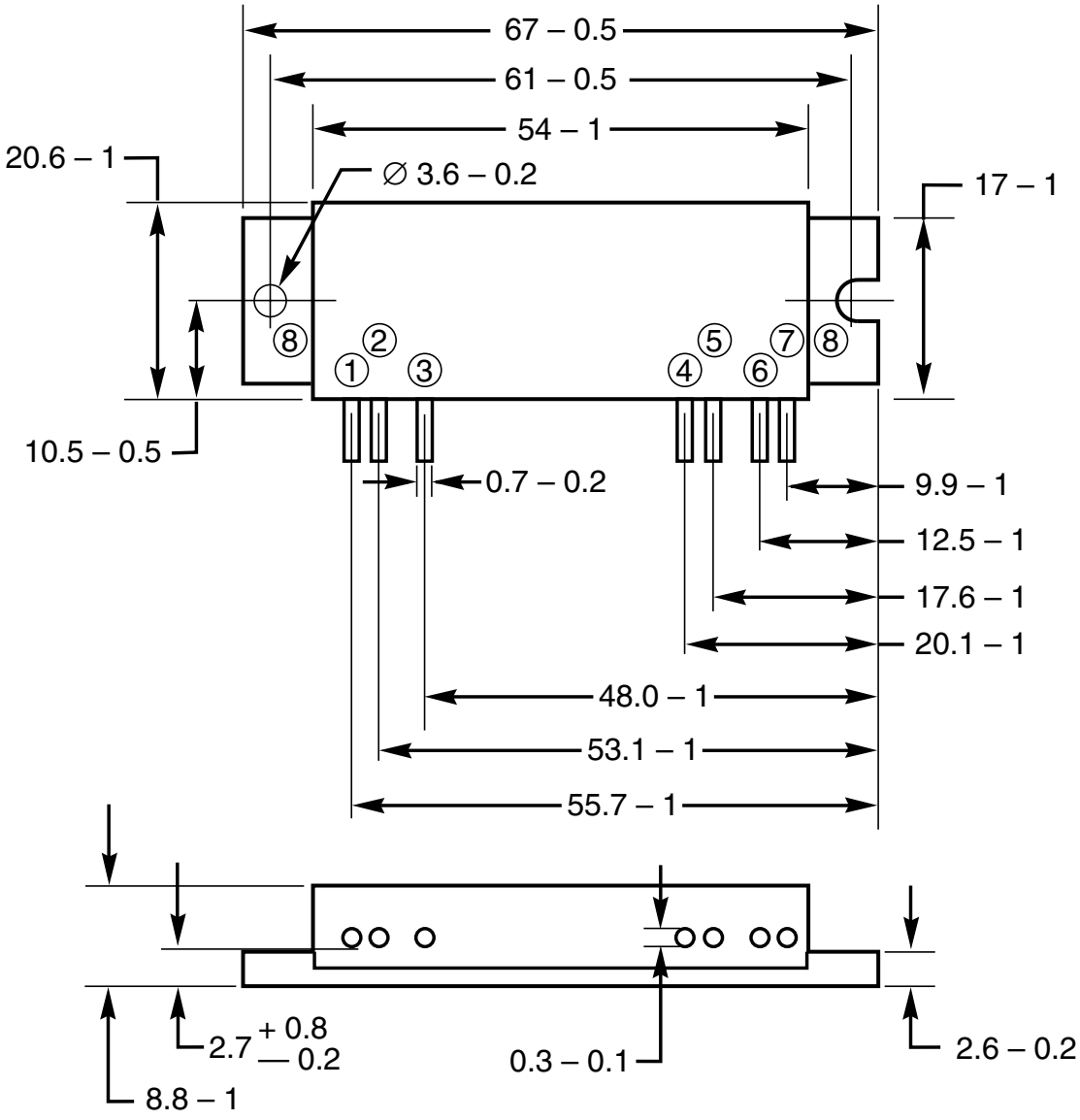
H17



PIN:

① INPUT
② V_{CC2}
③ V_{CC2}
④ OUTPUT
⑤ GND

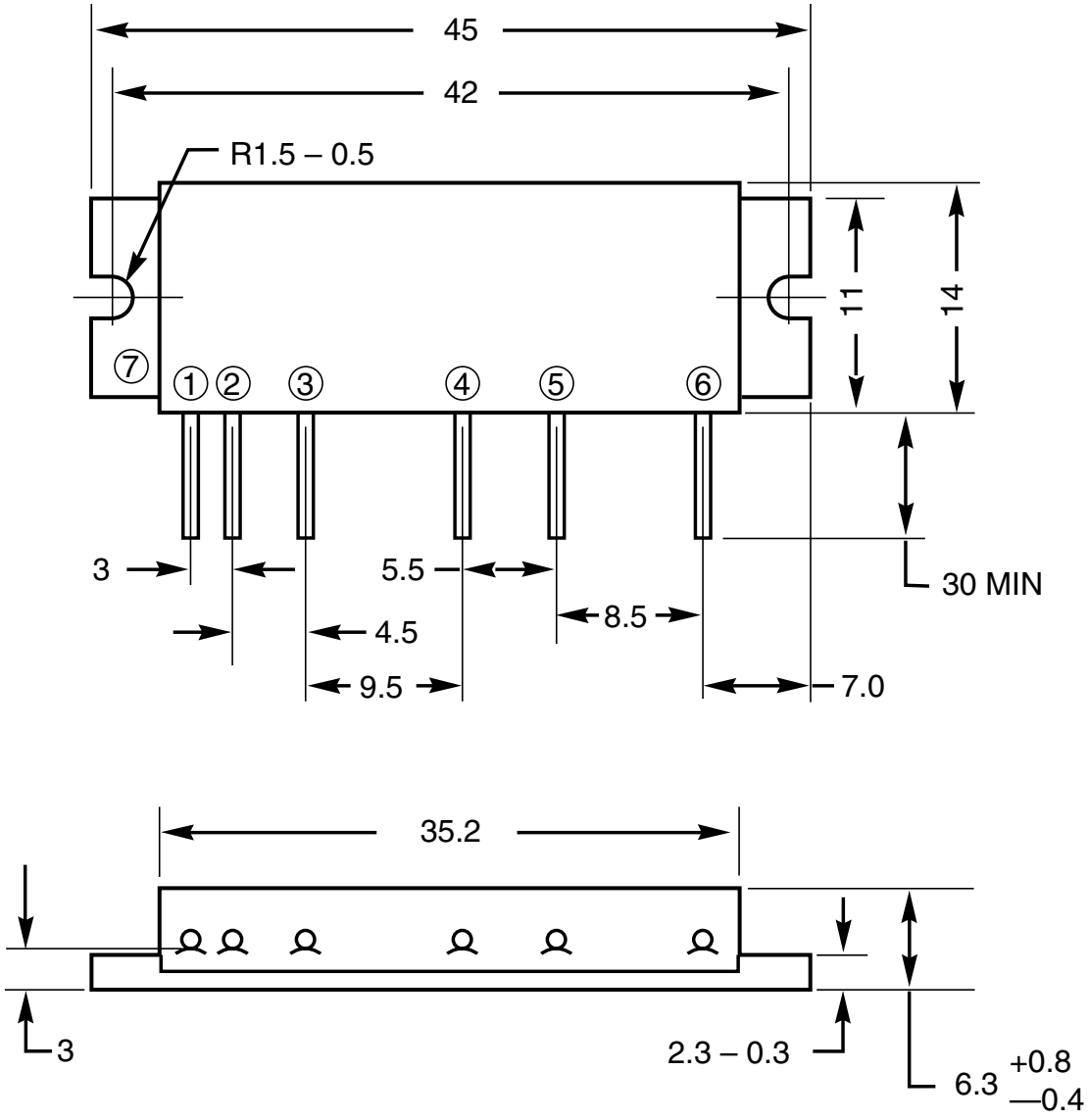
H18



PIN:

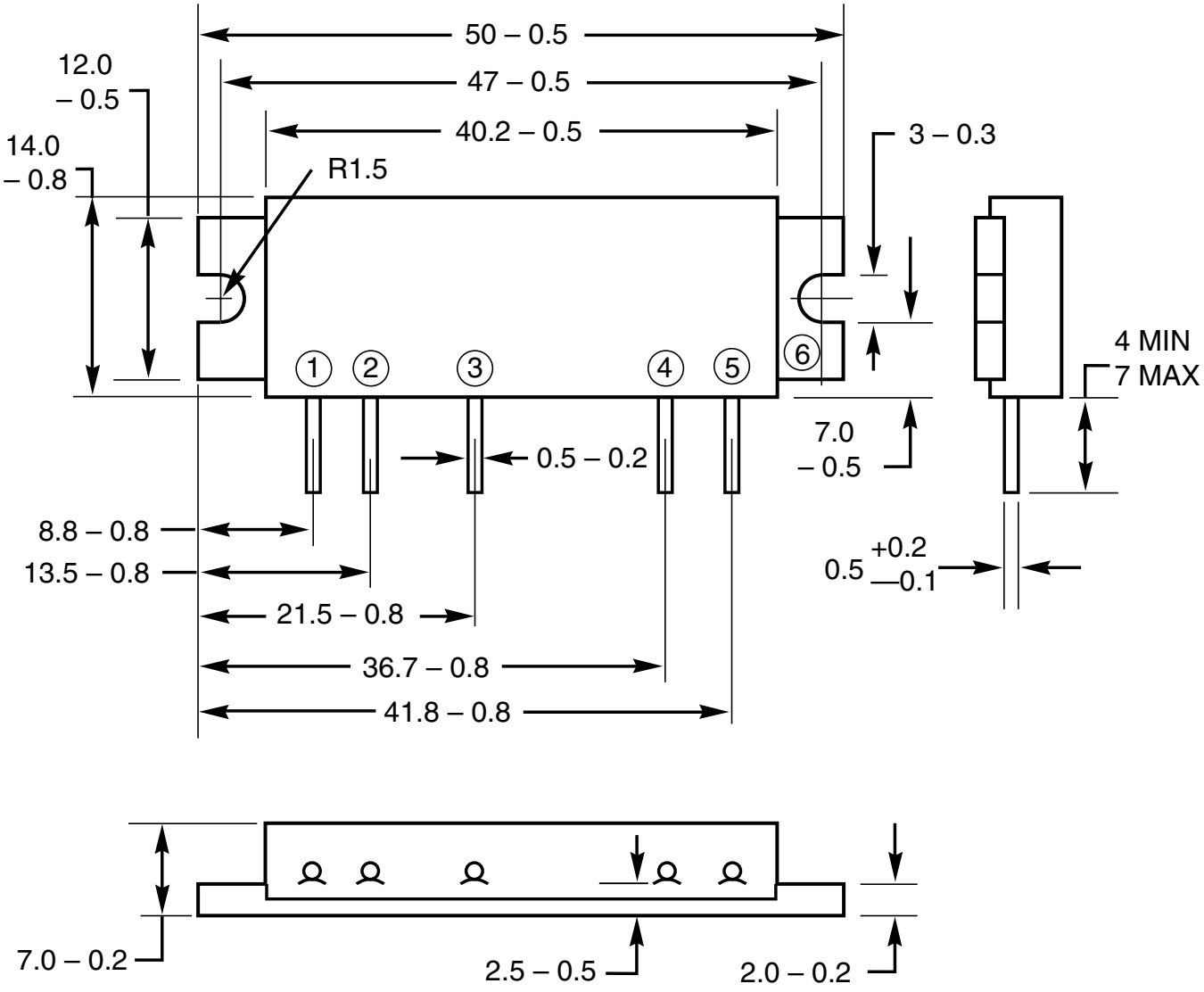
① OUTPUT	⑤ V_{CC1}
② GND	⑥ GND
③ V_{CC2}	⑦ INPUT
④ GND	⑧ GND

H24



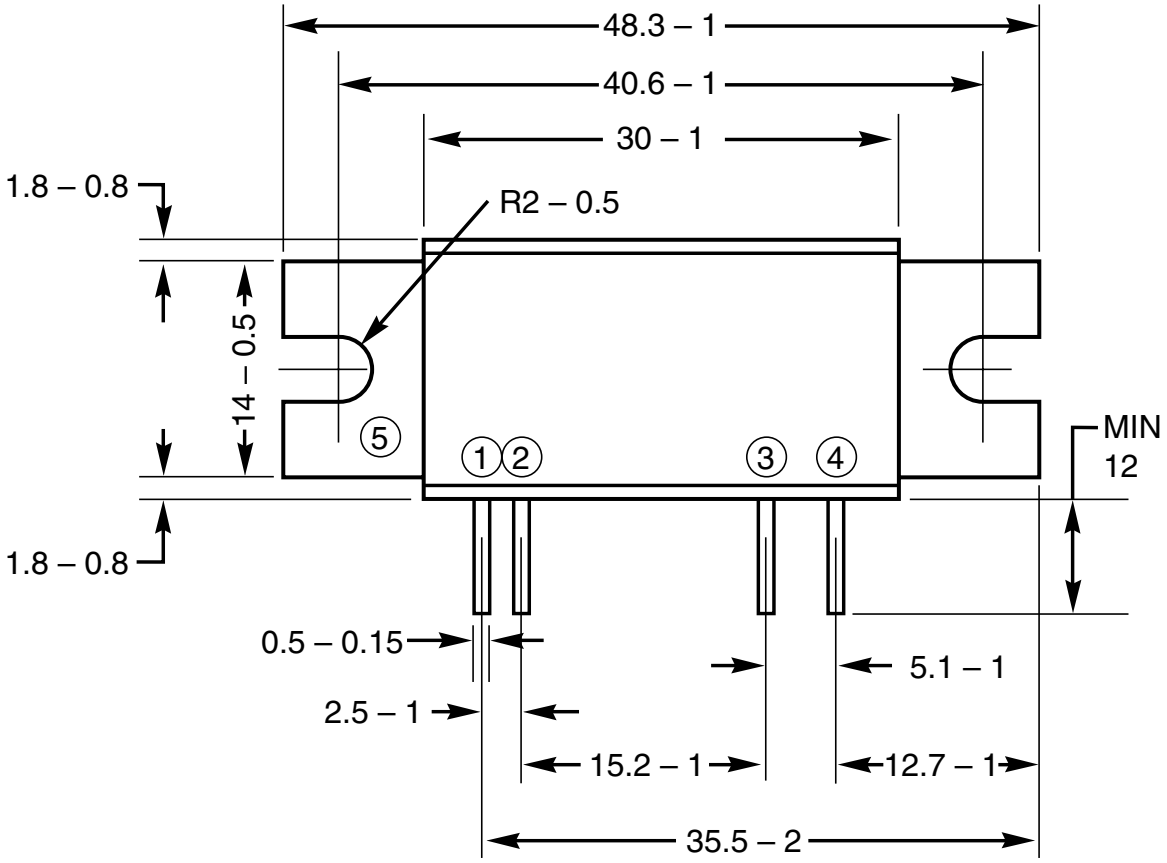
① OUTPUT
② V_{G1}
③ V_{D1}
④ V_{G2}
⑤ V_{D2}
⑥ OUTPUT
⑦ GND

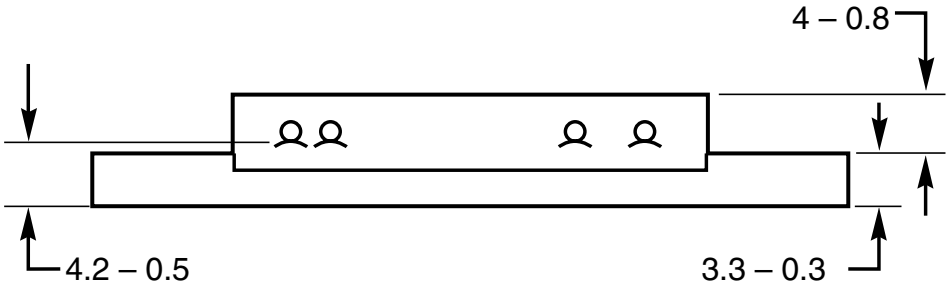
H25



① INPUT
② V_{CC1}
③ V_{CC2}
④ V_3
⑤ OUTPUT
⑥ GND

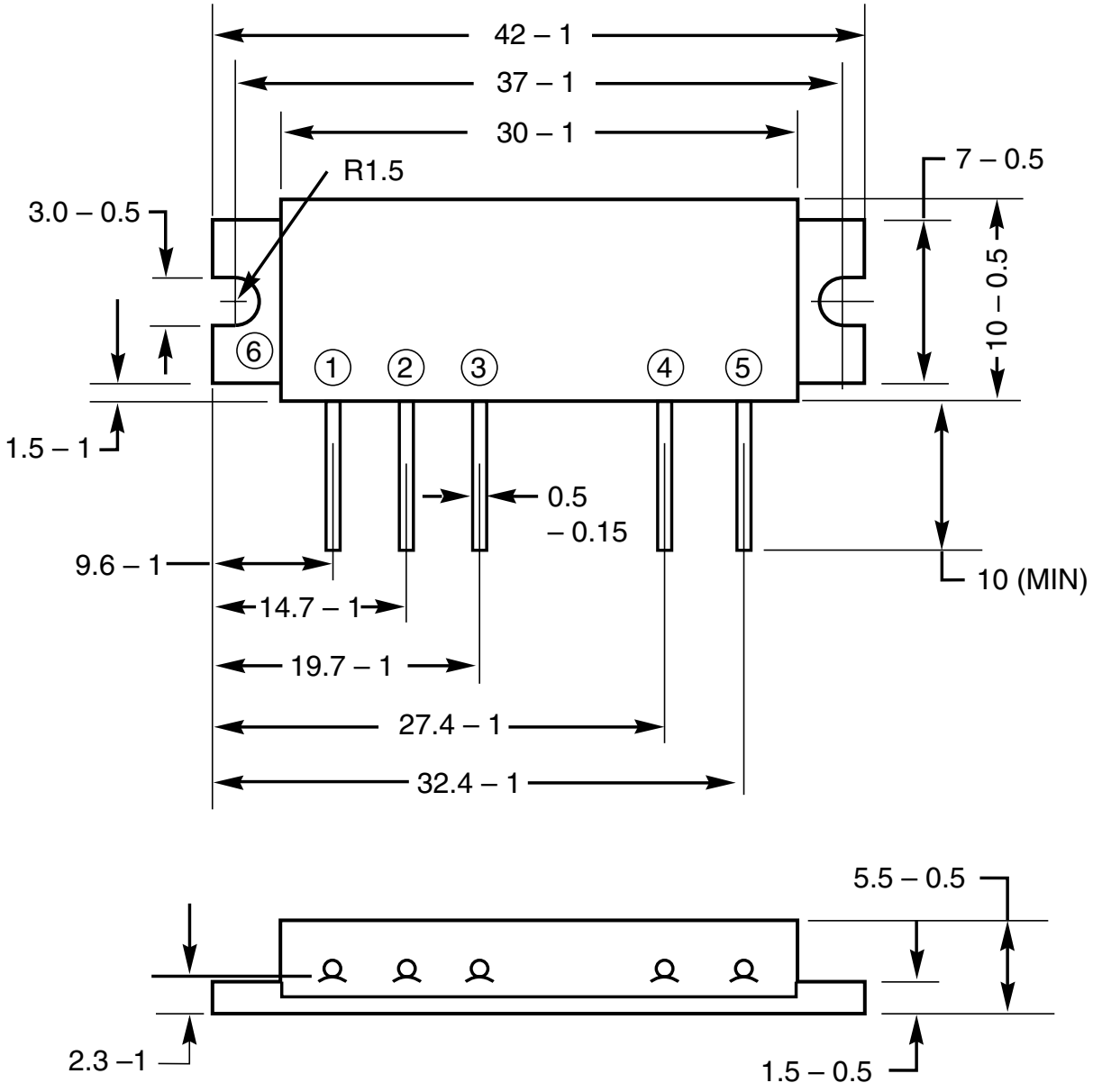
H26





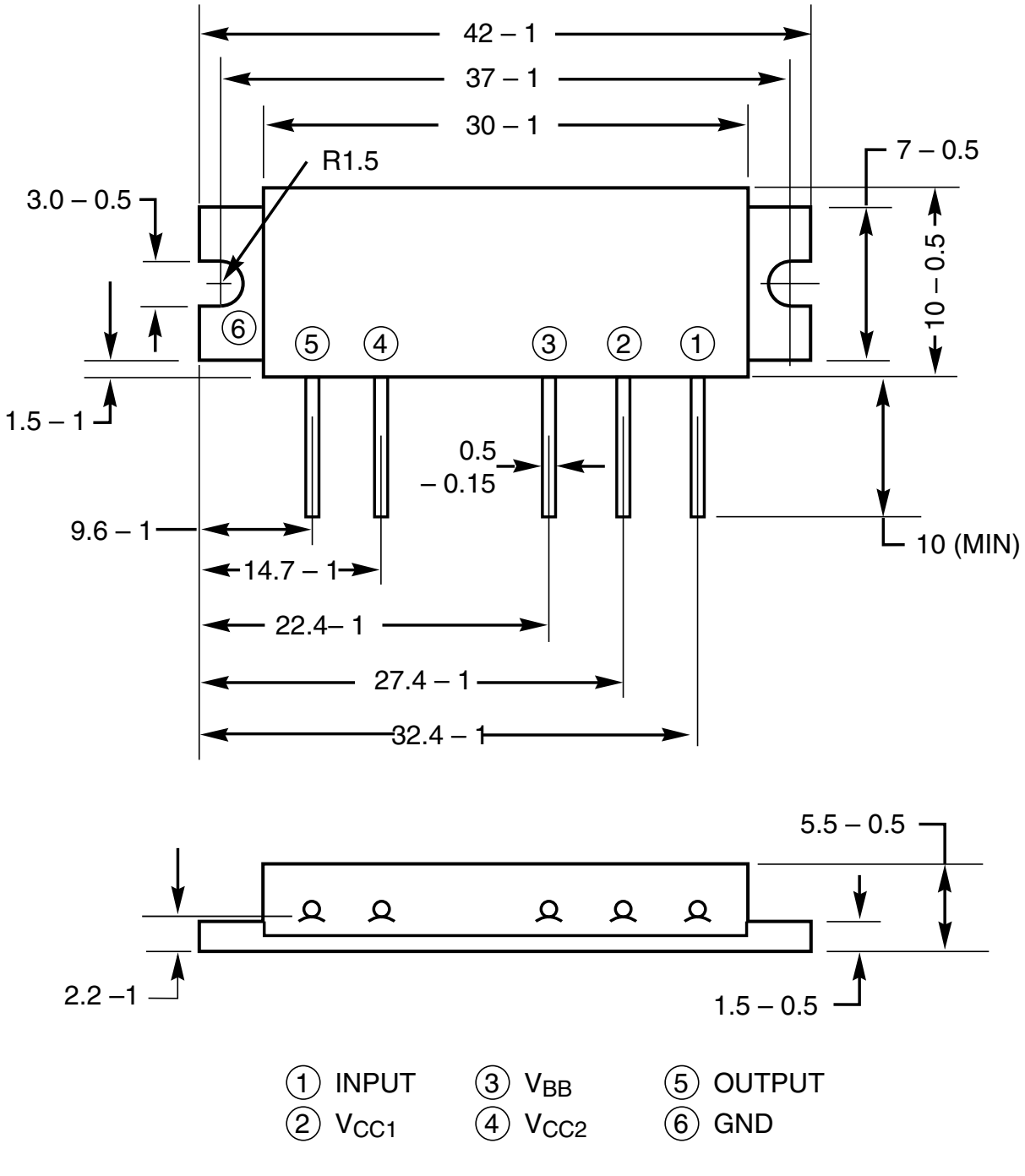
① INPUT ② V_{CC1} ③ V_{CC2} ④ OUTPUT ⑤ GND

H27



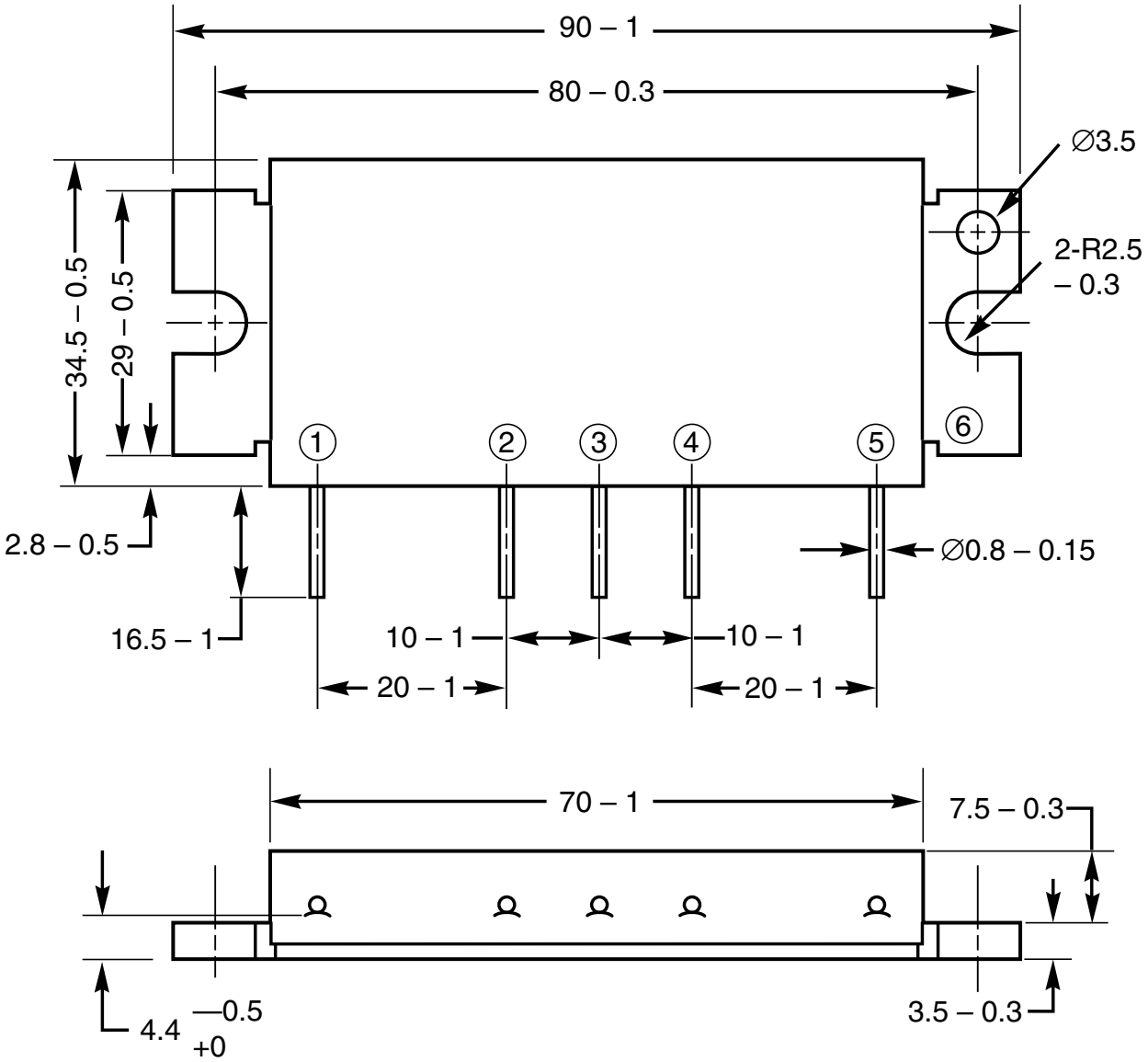
① INPUT ③ V_{BB} ⑤ OUTPUT
② V_{CC2} ④ V_{CC1} ⑥ GND

H27R



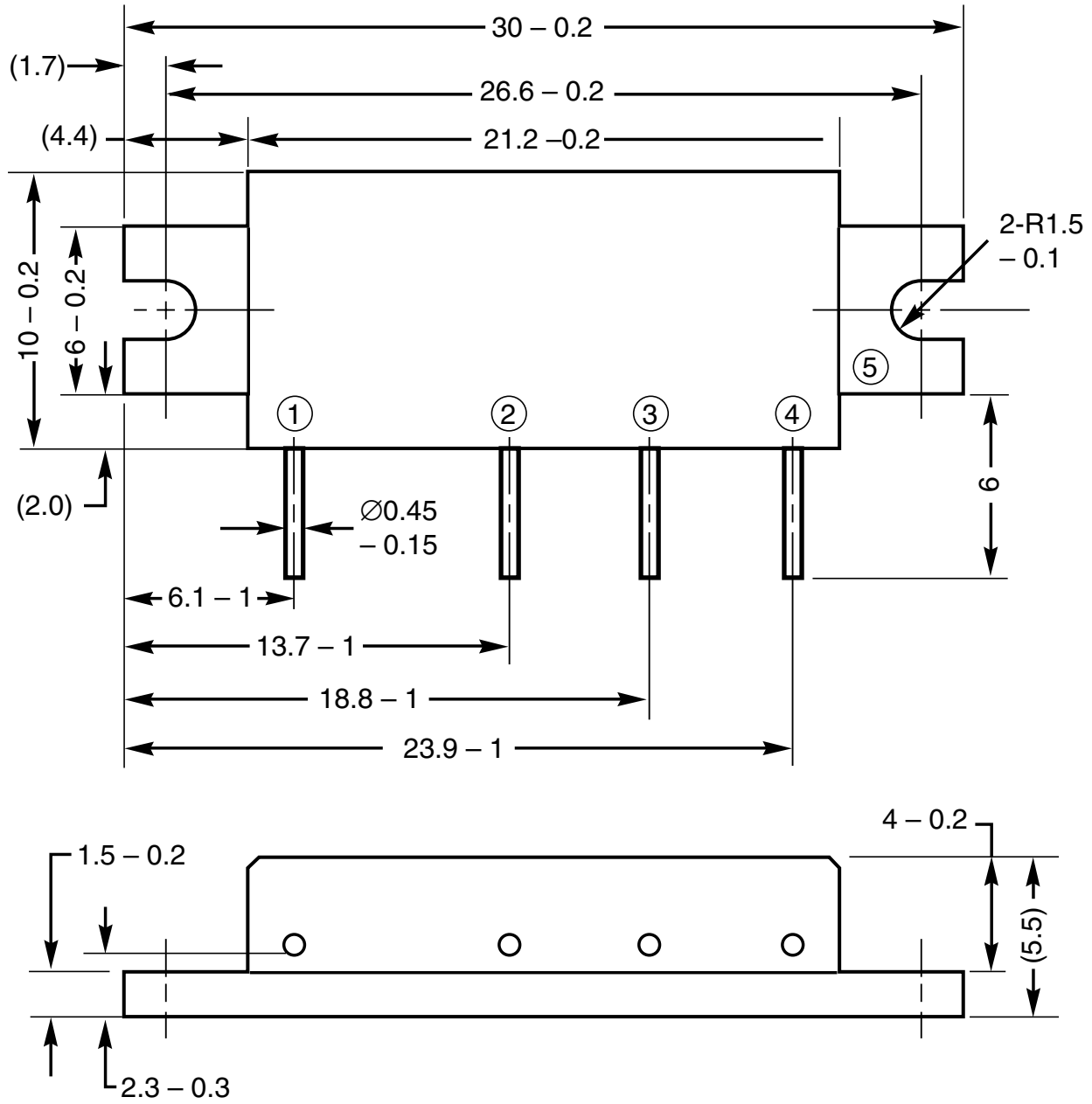
① INPUT ③ V_{BB} ⑤ OUTPUT
② V_{CC1} ④ V_{CC2} ⑥ GND

H28



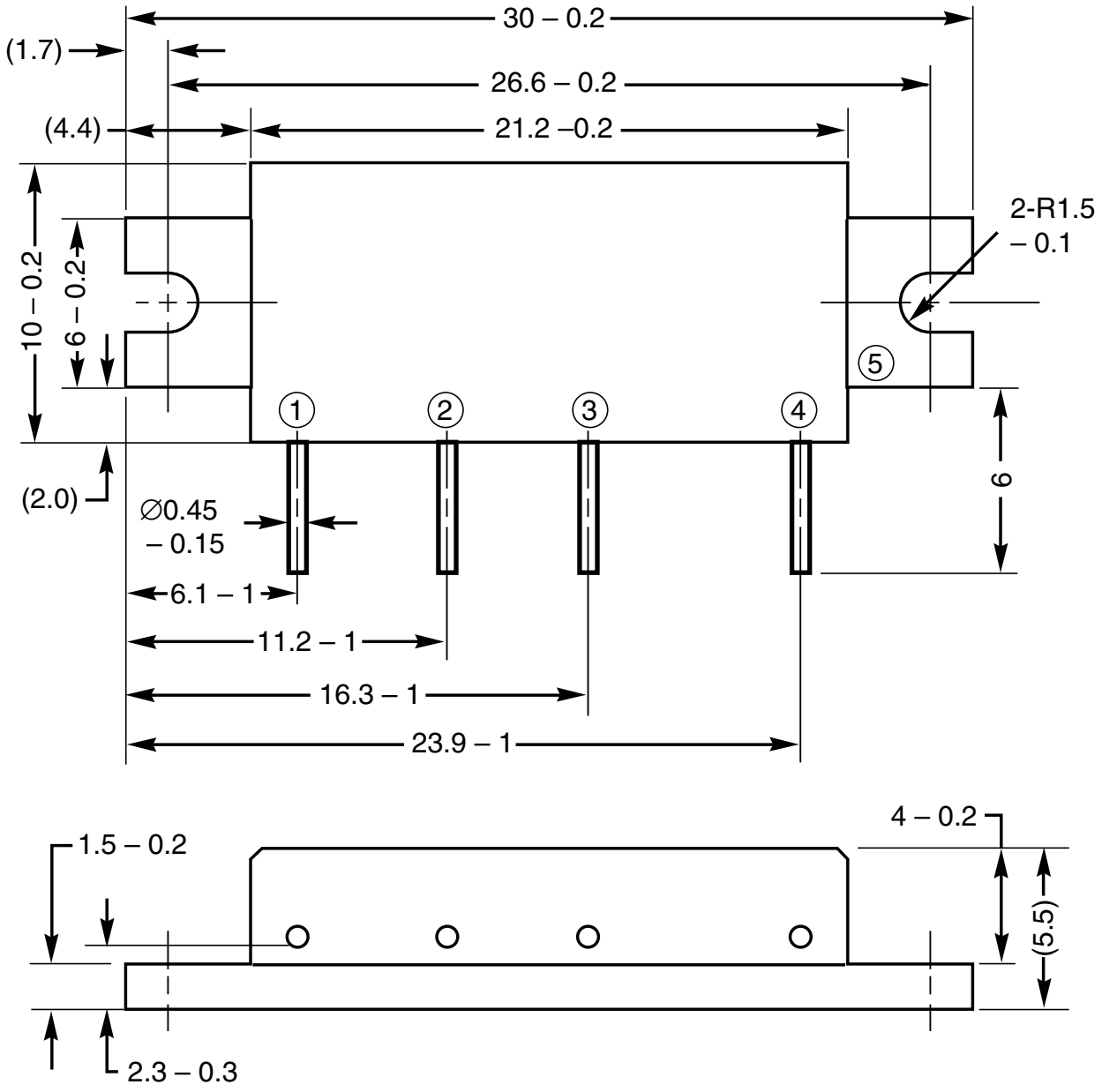
① P_{IN} : RF INPUT
② V_{CC1}: 1st DC SUPPLY
③ V_{BB} : BASE BIAS SUPPLY
④ V_{CC2}: 2nd DC SUPPLY
⑤ P_O : RF OUTPUT
⑥ GND : FIN

H46



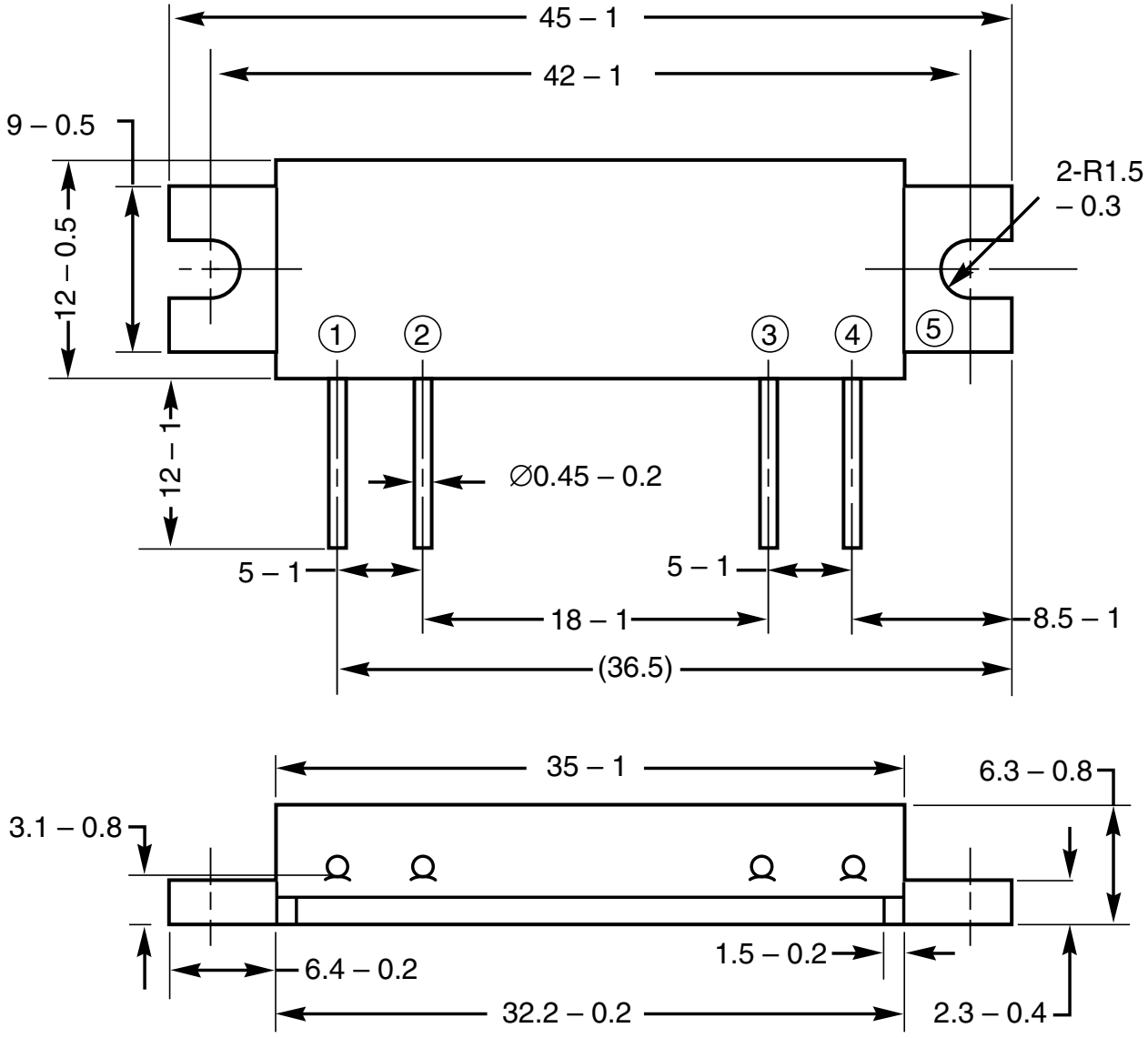
① P_{IN} : RF INPUT
② V_{GG} : GATE BIAS SUPPLY
③ V_{DD} : DRAIN BIAS SUPPLY
④ P_O : RF OUTPUT
⑤ GND : FIN

H47



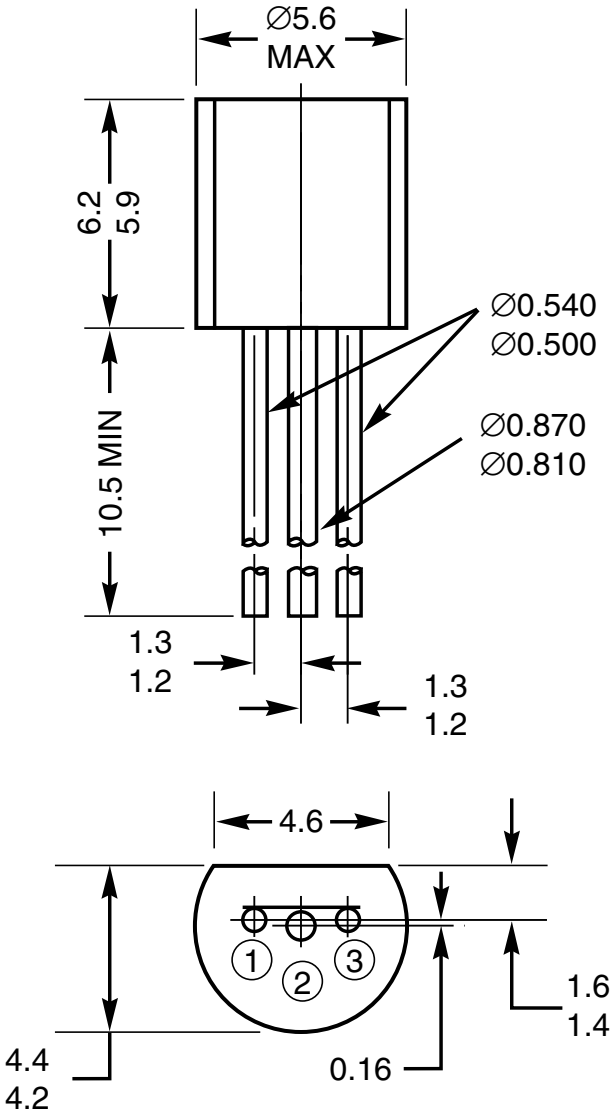
① P_O : RF OUTPUT
② V_{DD} : DRAIN BIAS SUPPLY
③ V_{GG} : GATE BIAS SUPPLY
④ P_{IN} : RF INPUT
⑤ GND : FIN

H50



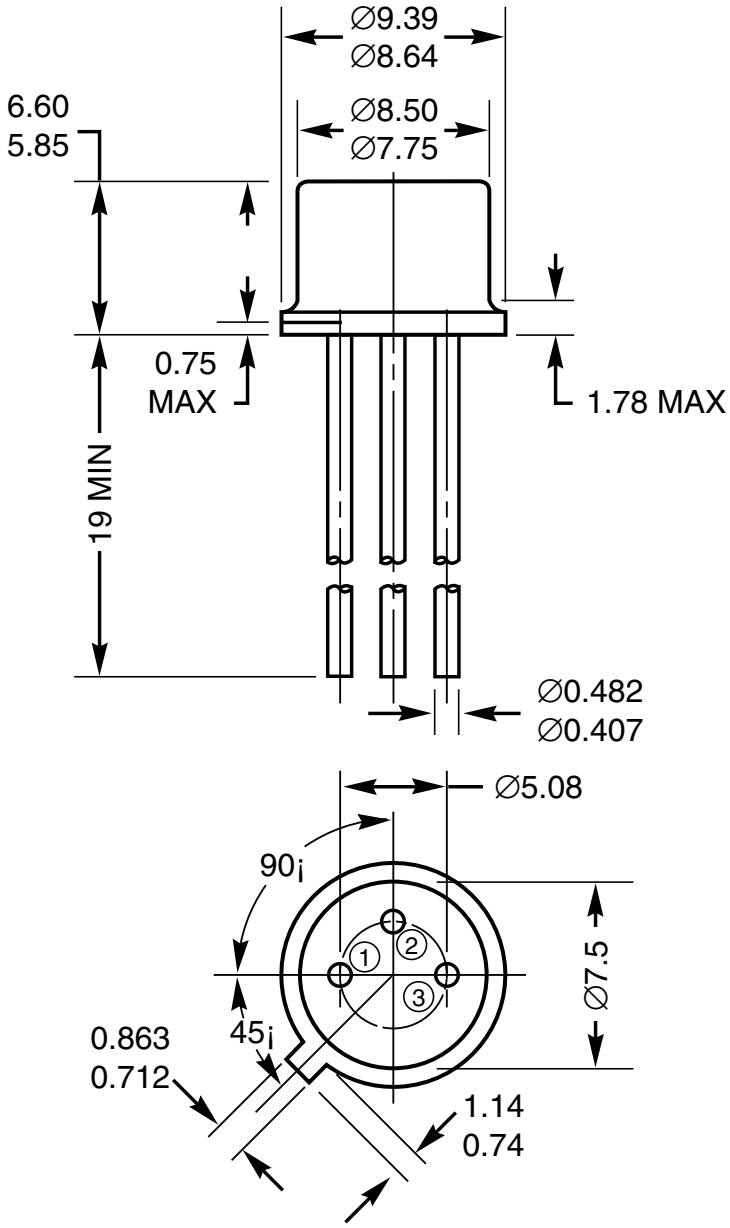
① P_{IN} : RF INPUT
② V_{GG} : GATE BIAS SUPPLY
③ V_{DD} : DRAIN BIAS SUPPLY
④ P_O : RF OUTPUT
⑤ GND : FIN

T-1B



① EMITTER
② COLLECTOR
③ BASE

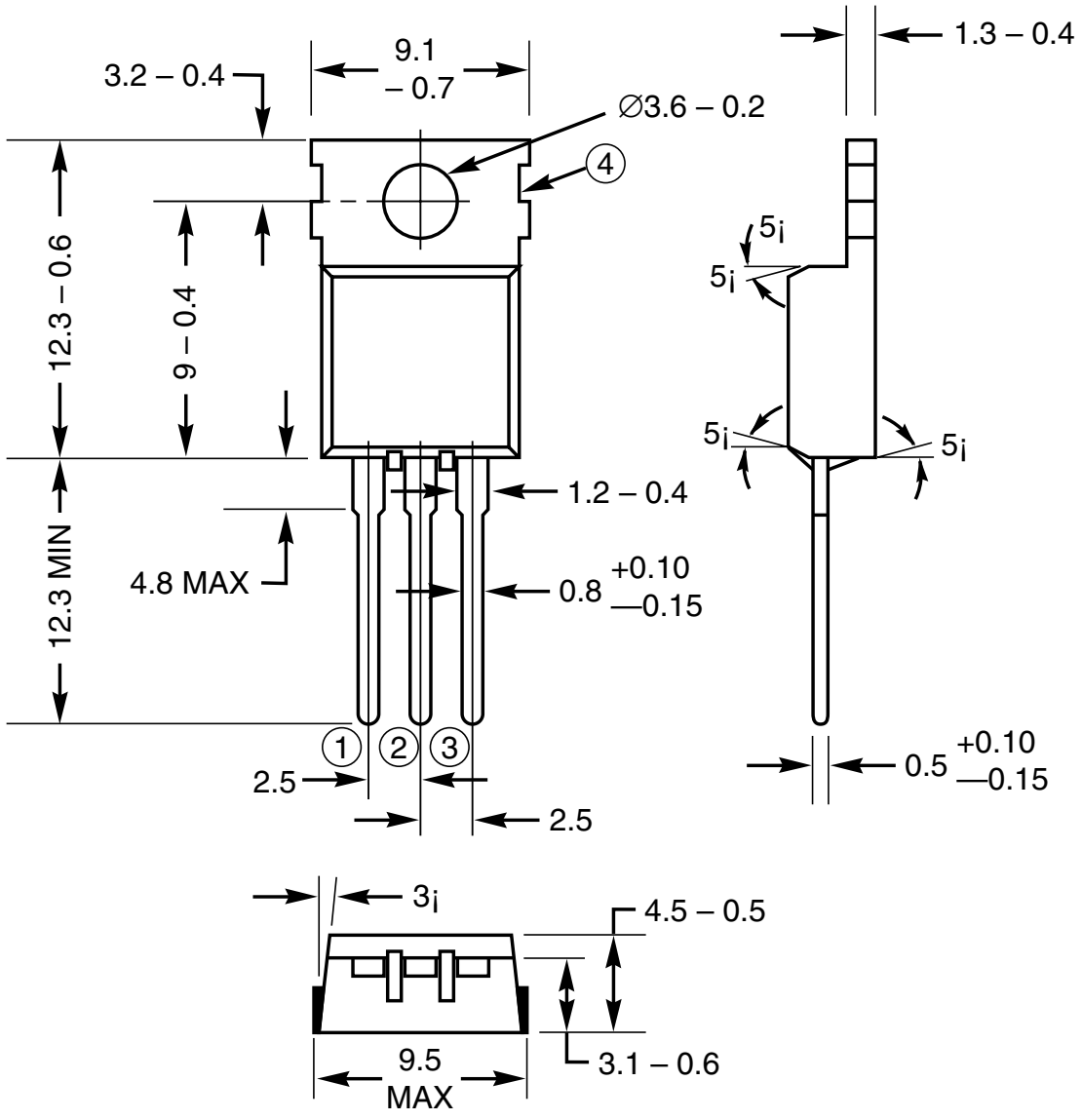
T-8,C,E



① EMITTER
② BASE
③ COLLECTOR JEDEC: TO-39

NOTE T-8C: COLLECTOR ELECTRODE IS CONNECTED WITH CASE.
T-8E: EMITTER ELECTRODE IS CONNECTED WITH CASE.

T-30,E



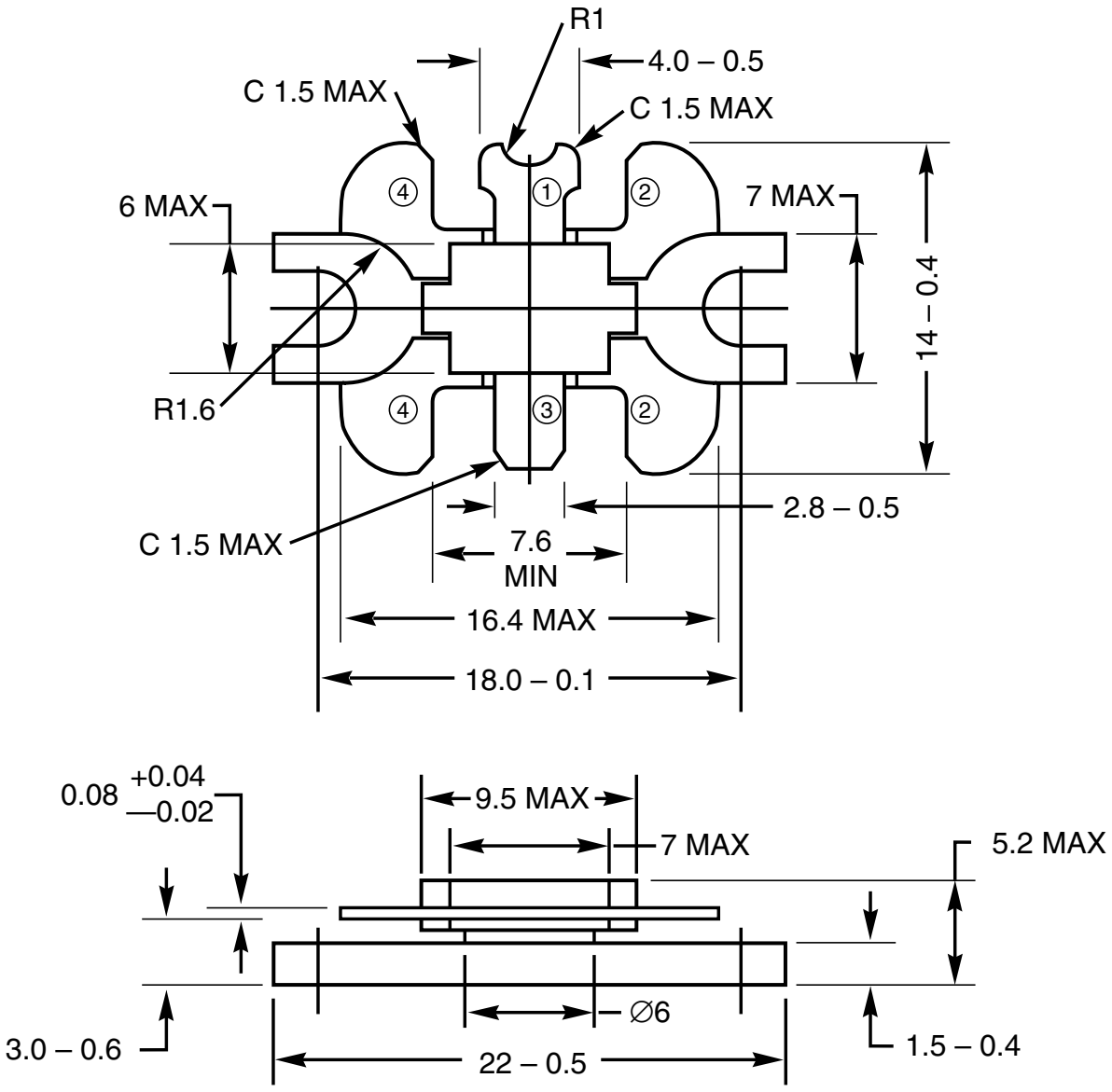
T-30

① BASE
② COLLECTOR (FIN)
③ EMITTER
④ FIN (COLLECTOR)

T-30E

① BASE
② EMITTER (FIN)
③ COLLECTOR
④ FIN (EMITTER)

T-31,B,E



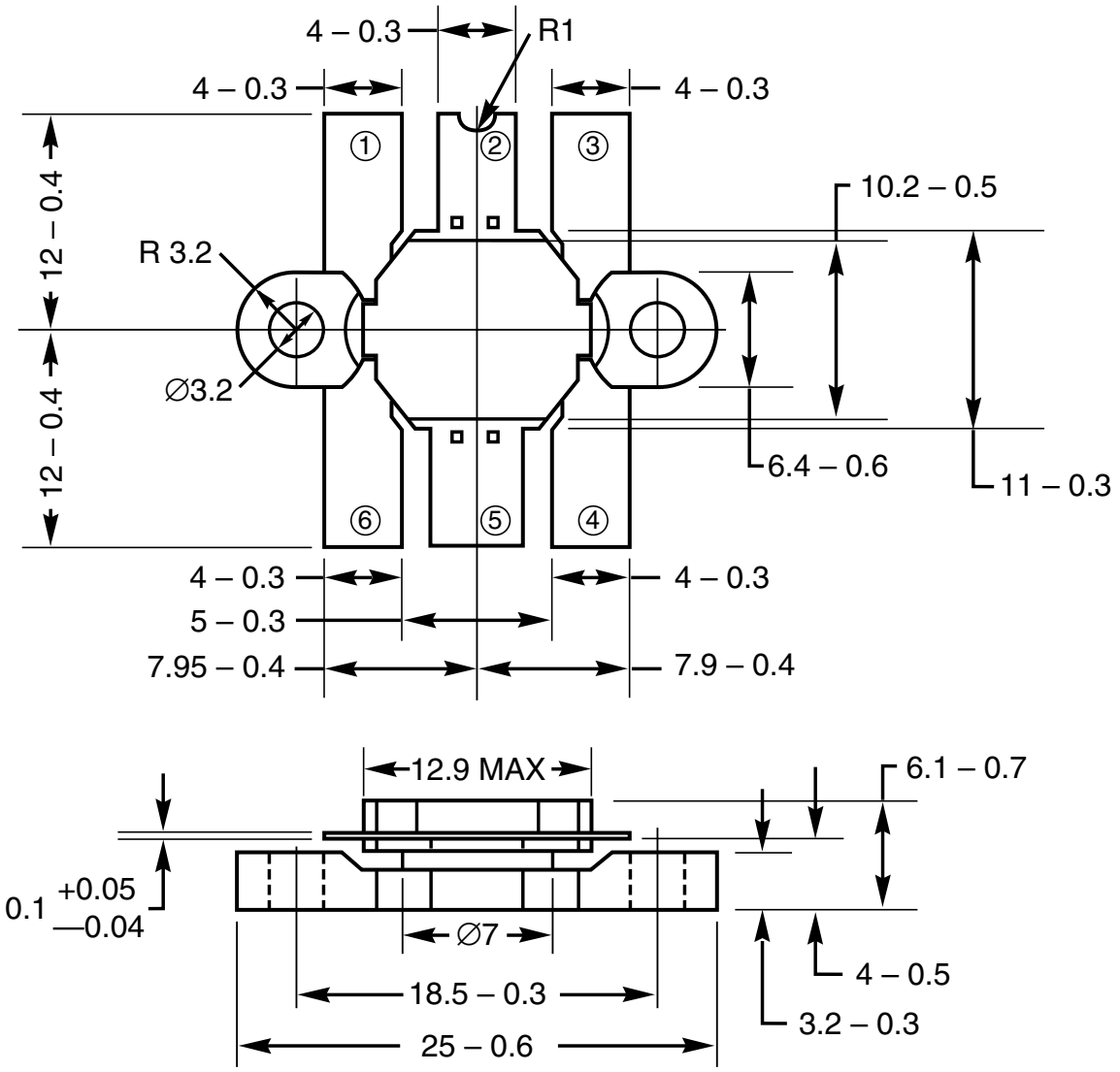
T-31B

① COLLECTOR
② BASE (FLANGE)
③ EMITTER
④ BASE (FLANGE)

T-31E

① COLLECTOR
② EMITTER (FLANGE)
③ BASE
④ EMITTER (FLANGE)

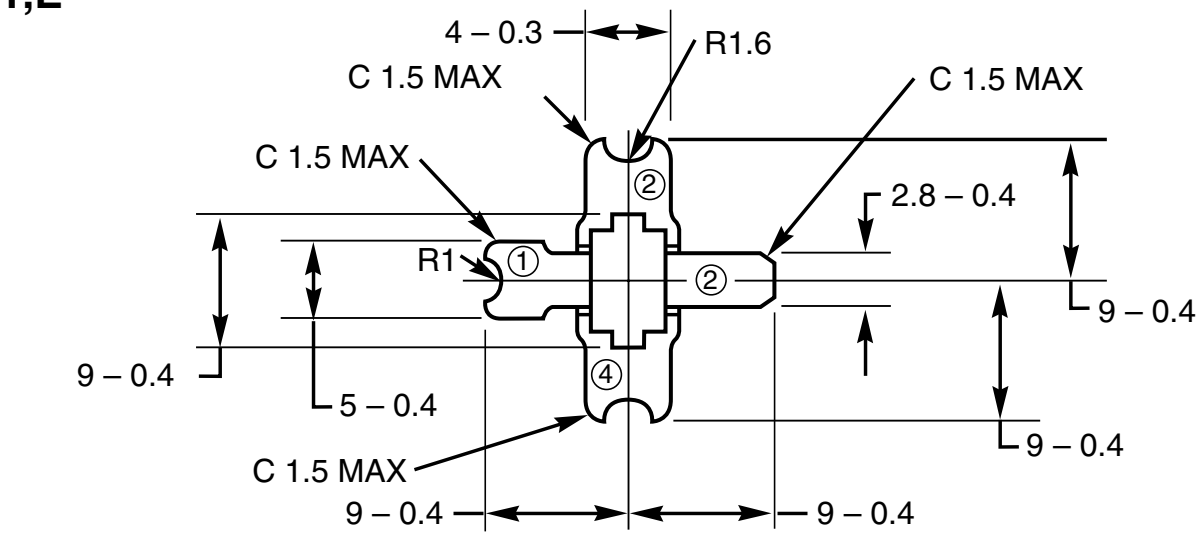
T-40,E

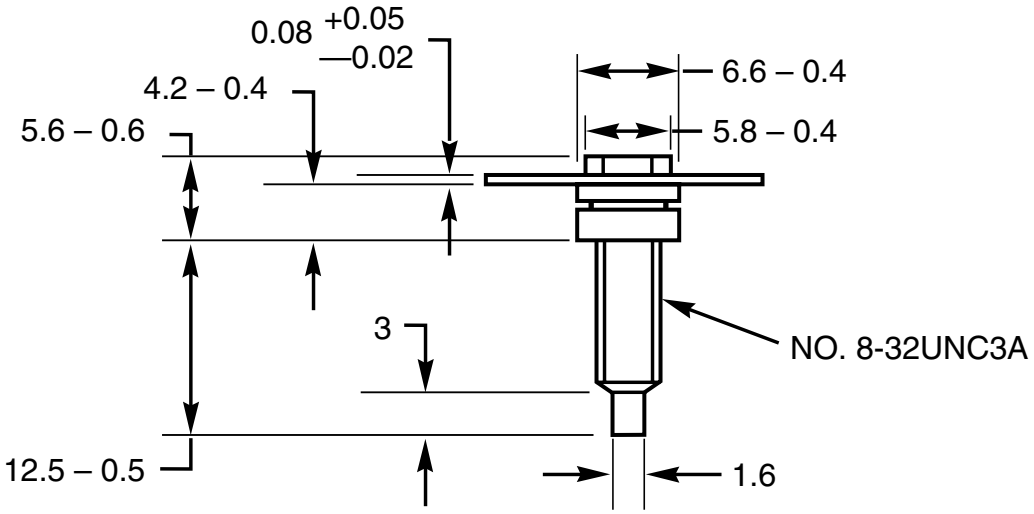


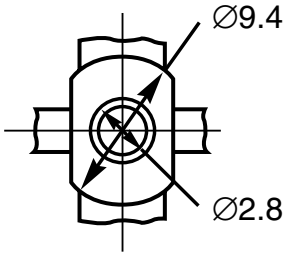
① COLLECTOR
② EMITTER
③ BASE
④ EMITTER

NOTE T-40: ALL ELECTRODES ARE ISOLATED FROM FLANGE.
T-40E: EMITTER ELECTORDES ARE CONNECTED WITH FLANGE.

T-41,E



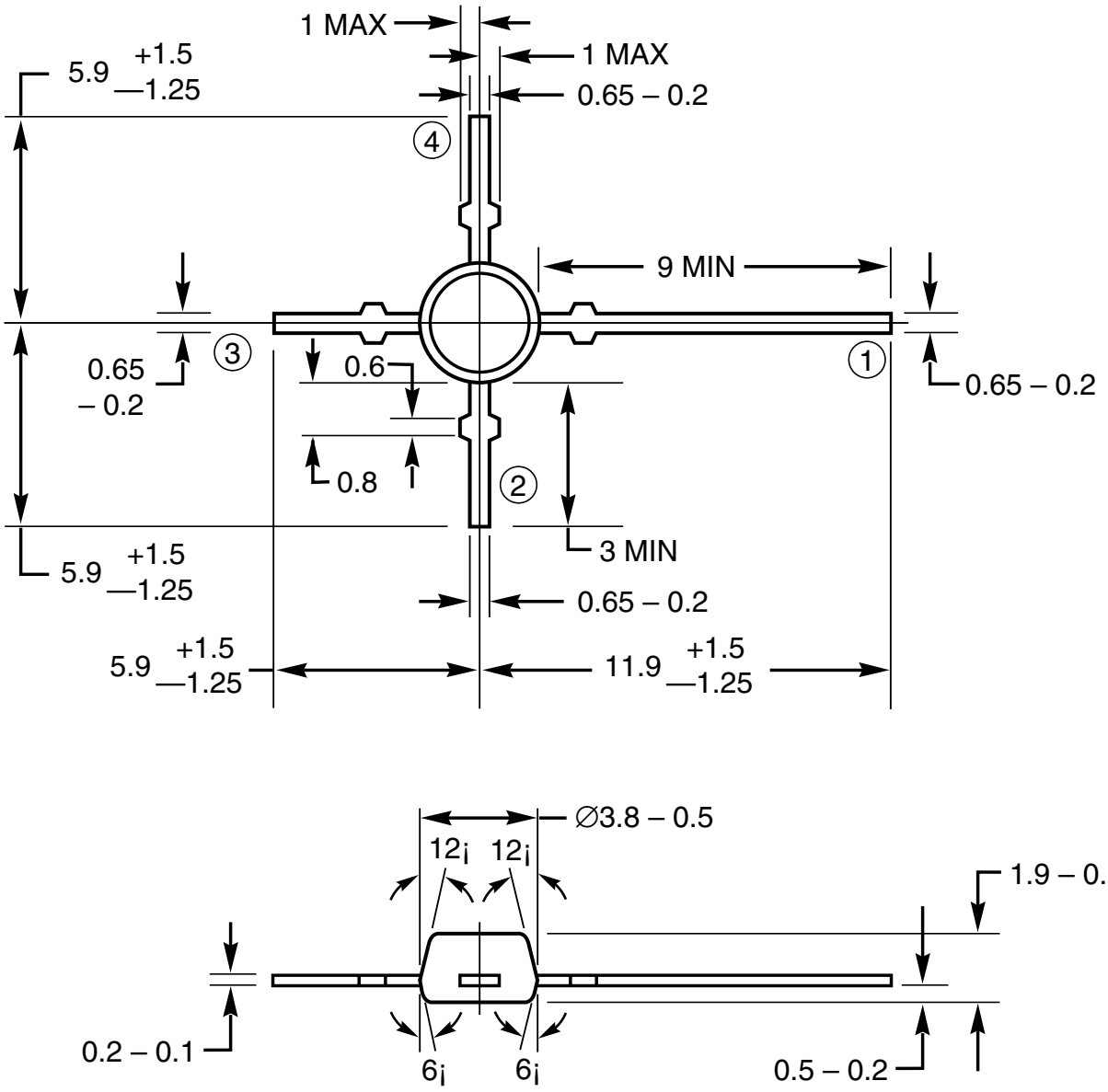




① COLLECTOR
② EMITTER
③ BASE
④ EMITTER

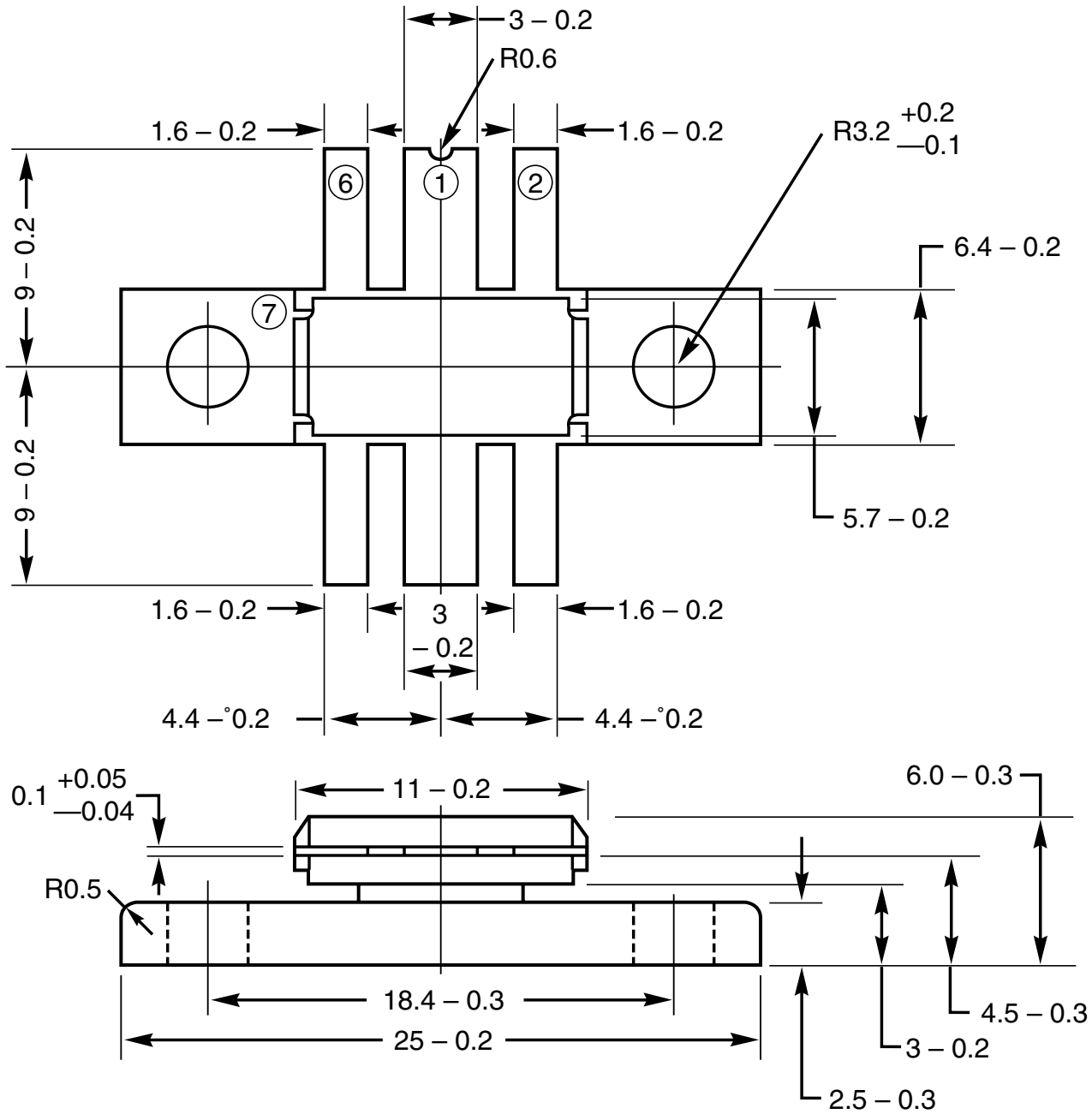
NOTE T-41: ALL ELECTRODES ARE ISOLATED FROM FLANGE.
T-41E: EMITTER ELECTORDES ARE CONNECTED WITH FLANGE.

T-43



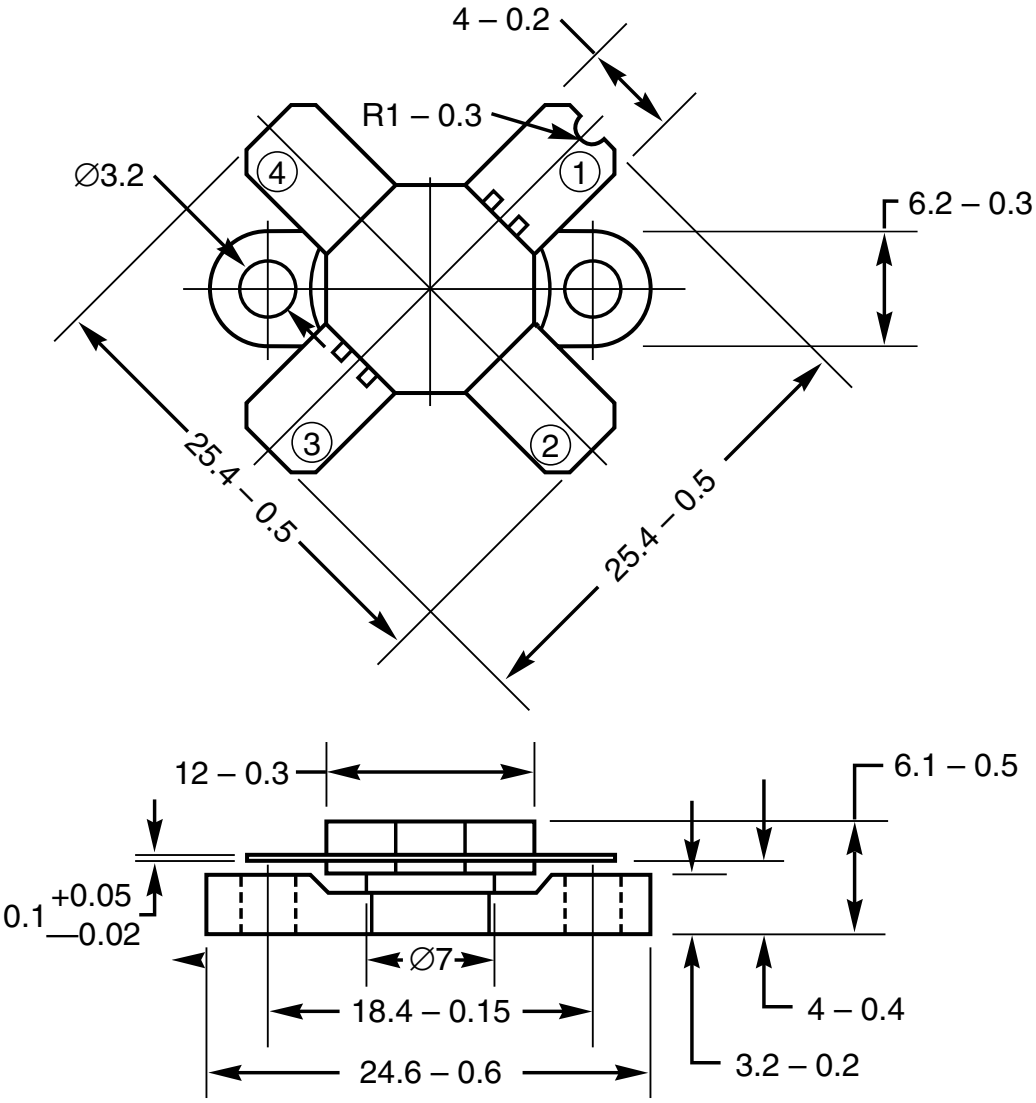
① COLLECTOR
② EMITTER
③ BASE
④ EMITTER

T-44



① COLLECTOR
② BASE (FLANGE)
③ EMITTER
④ BASE (FLANGE)

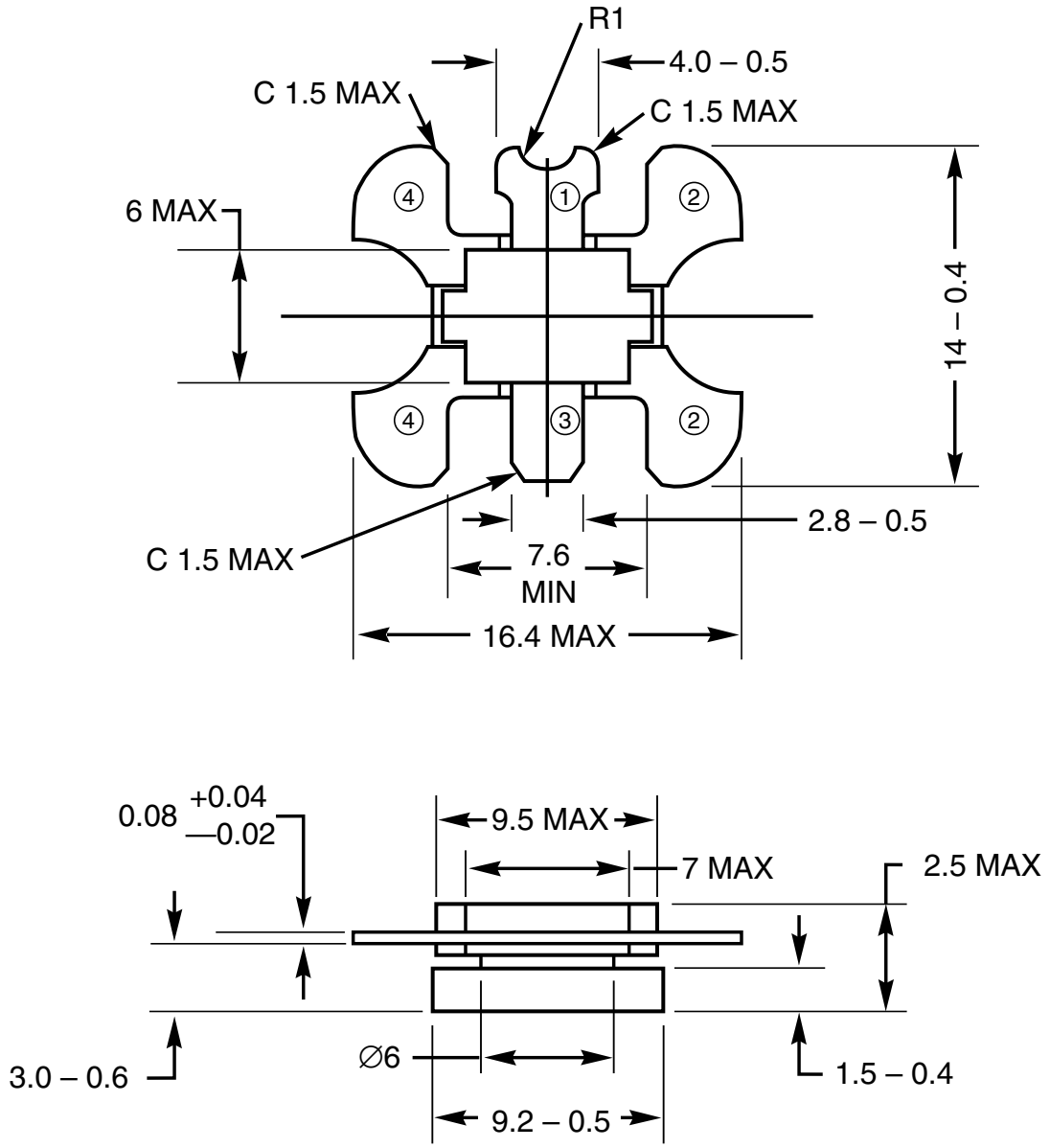
T-45,E



① COLLECTOR
② EMITTER
③ BASE
④ EMITTER

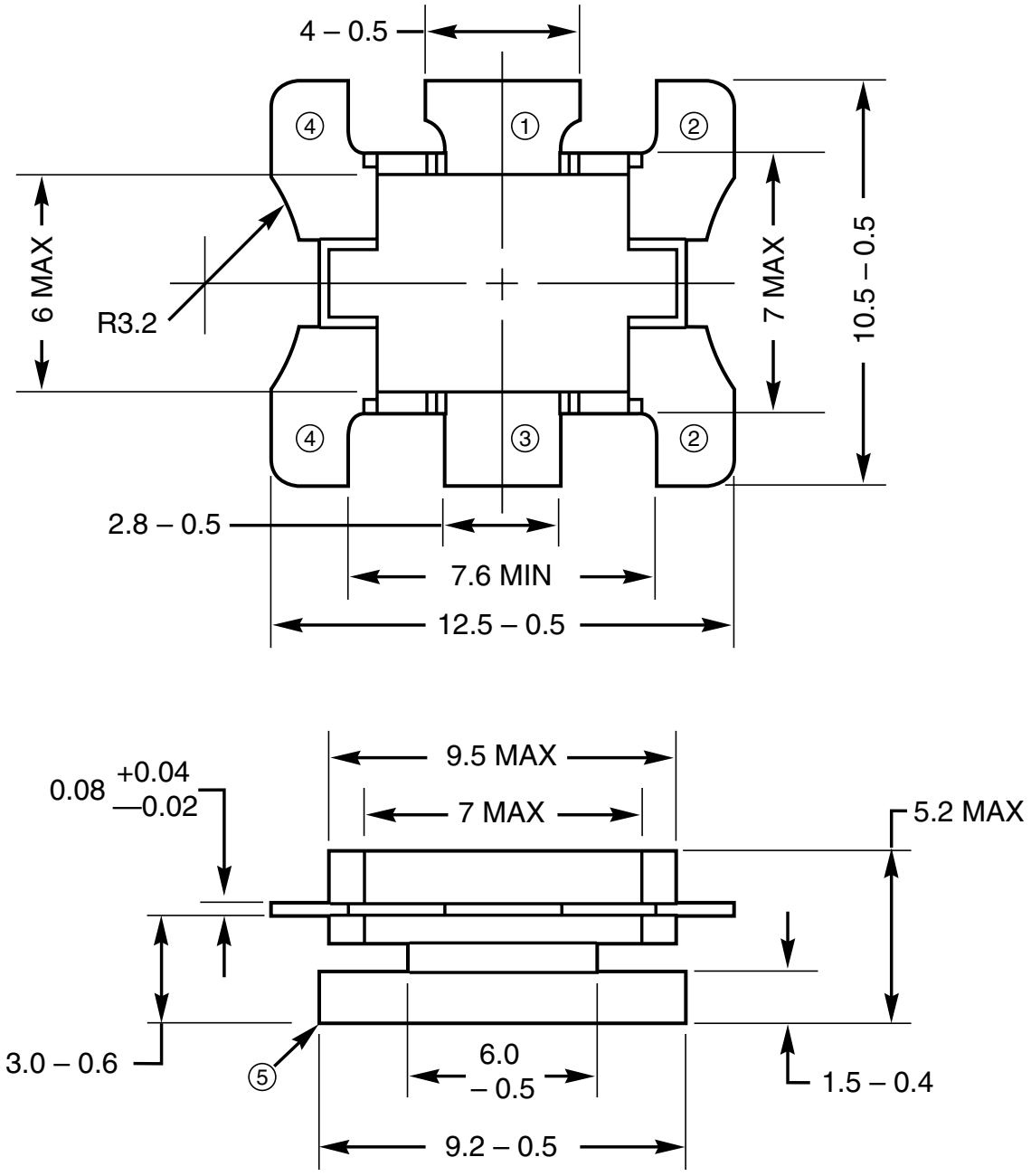
NOTE T-45: ALL ELECTRODES ARE ISOLATED FROM FLANGE.
T-45E: EMITTER ELECTORDES ARE CONNECTED WITH FLANGE.

T-46



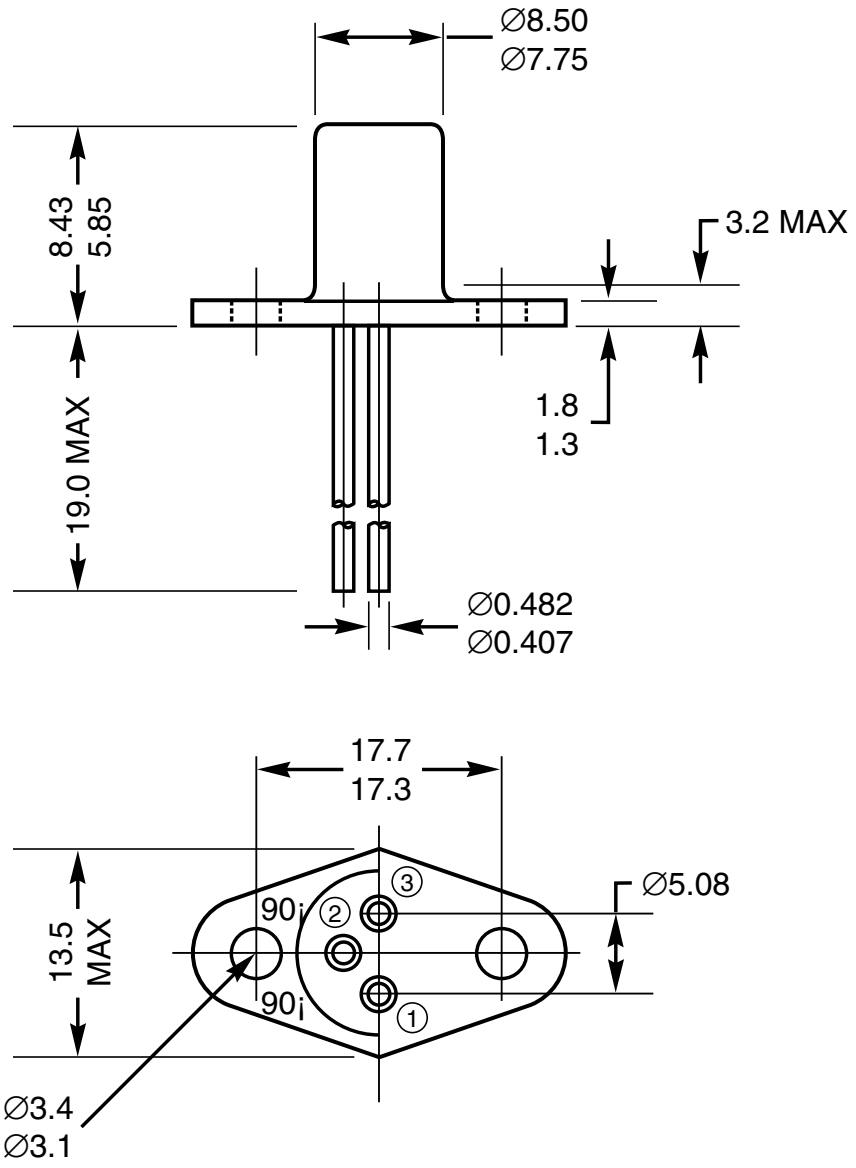
① COLLECTOR
② EMITTER (FLANGE)
③ BASE
④ EMITTER (FLANGE)

T-47



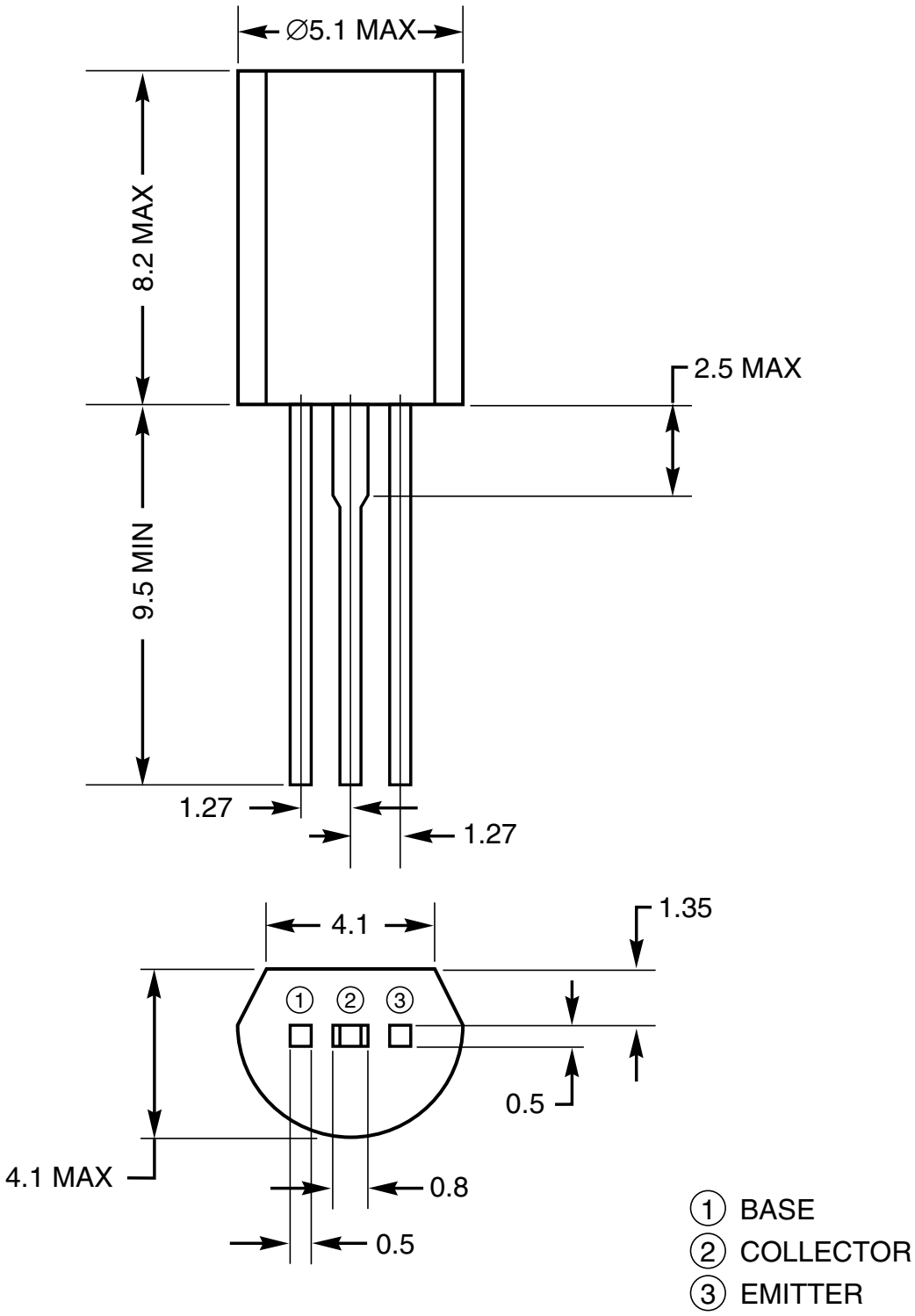
① COLLECTOR
② EMITTER (FLANGE)
③ BASE
④ EMITTER (FLANGE)
⑤ FIN (EMITTER)

TC-17

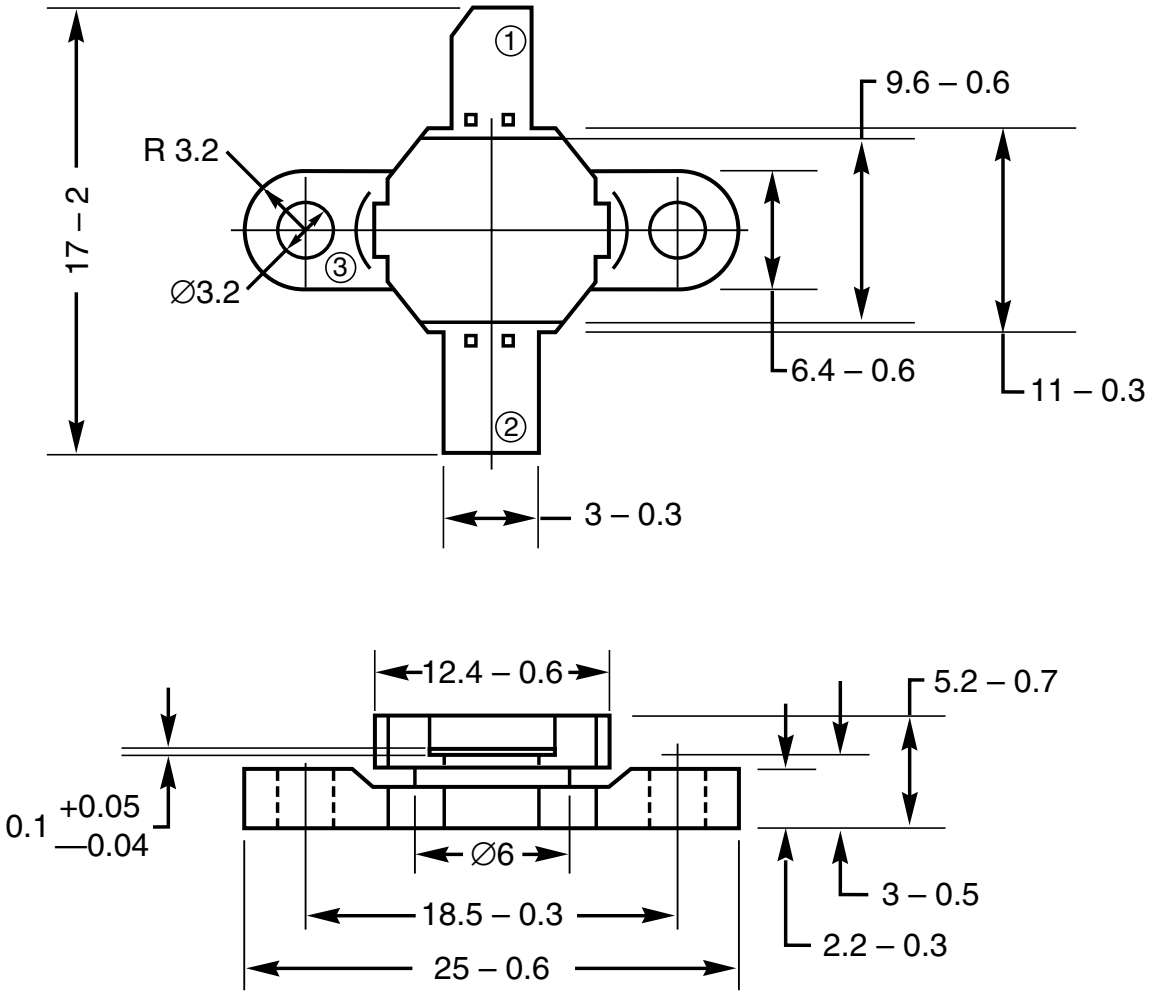


① EMITTER (CASE)
② BASE
③ COLLECTOR

TO-92L


∅5.1 MAX
8.2 MAX
2.5 MAX
9.5 MIN
1.27
1.27
4.1
1.35
① ② ③
0.5
4.1 MAX
0.8
0.5
① BASE
② COLLECTOR
③ EMITTER

X-139



① COLLECTOR
② EMITTER
③ BASE (FLANGE)